

GPS Receivers for syn1588® NICs

Version 1.17.1 - October 2023

Abstract

The syn1588® PCIe NIC as well as the syn1588® Dual NIC allow the connection of an external GPS receiver that provides the absolute time for IEEE1588 master operations. This application note briefly describes the basic setup procedure as well as the requirements for selecting an appropriate GPS receiver.

Using a GPS Receiver

Using an external GPS receiver to supply an absolute time reference for a syn1588® NIC is a simple task. One just requires two connections:

- the 1PPS signal
- the serial NMEA data stream

The following figure shows the basic connection scenario when connecting a syn1588® NIC with a GPS receiver. Please note, while basically there is no difference between the basic functions of the syn1588® PCIe NIC and the syn1588® Dual NIC there are some specific limitations for the syn1588® Dual NIC due to the limited number of SMA IOs. Please check the Application Note AN0036 "Special considerations when using IOs of the syn1588® Dual NIC" for further details.

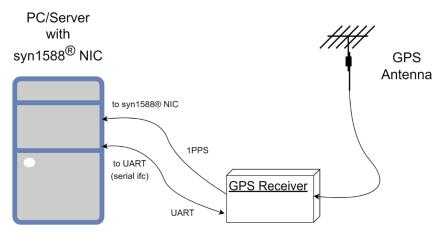


Figure 1 Basic connection scenario for a GPS receiver

The 1PPS signal provides the exact phase information while the serial data stream provides the absolute time information for each 1PPS event. The GPS receiver has to support the NMEA-0183 protocol (including the RMC messages).

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The following NMEA output example shows only a small part of the possible log files and additional messages. NMEA has its own version of essential gps pvt (position, velocity, time) data. It is called RMC.

GPRMC, 123519, A, 4807.038, N, 01131.000, E, 022.4, 084. (, 230317) 003.1, W, F*6A

The data needed by eSync are in this example:

123519 = time of day 12:35:19 UTC 230317 = date of day 23 of march 2017

If the seconds in time of day have the value 60 a leap second will be applied i.e. the utcOffset will be increased by 1.

From the software point of view there is the syn1588® PTP Stack required as well as the eSync utility. Both software come with every syn1588® NIC.

The basic sequence of invoking the software is:

- invoke the syn1588® PTP Stack first instructing to act as PTP Master
- wait some seconds
- invoke eSync informing which SMA IO connector and UART shall be used for communication

Naturally, this sequence can be scripted to simply things. For a detailed explanation of both eSync and the syn1588® PTP Stack please check the syn1588® User Guide. The following eSync invocation shows a typical example:

```
sudo ./eSync -p 4 -c ttyUSB0 -b 4800 -v2 -s -d 0
```

The command line options used specify the following behavior:

- -p 4: use connector X4 for 1PPS signal
- -c ttyUSB0: use this (Linux) device for the serial interface
- -b 4800: select a baud rate of 4800
- -v2: set a verbosity level of 2 on the output
- -s: use shared memory to control/instruct the syn1588[®] PTP Stack
- -d 0: use card 0

A typical command output may look like this:

```
oregano@oregano:/opt/oregano/bin$ sudo ./eSync -p 4 -c ttyUSB0 -b 4800
2023-10-05 13:09:08.643711 [INFO
                                 ] [
                                                  ] syn1588(R) eSync - External
Synchronization Engine
2023-10-05 13:09:08.643749 [INFO
                                                  ] Build date: 2023-10-
                                  ] [
01T08:59:39 - v1.17-0-g0e870b57c
2023-10-05 13:09:08.643754 [INFO
                                  1 [
                                                  ] Copyright (c) Oregano
Systems - Design & Consulting GesmbH 2005-2023
2023-10-05 13:09:08.643758 [INFO
                                                  1 Confidential unpublished
                                  ] [
data - All rights reserved
2023-10-05 13:09:08.643776 [INFO
                                   1 [
                                                 ] Port 0: adding config "p" =
2023-10-05 13:09:08.643784 [INFO
                                   ] [
                                                  Port 0: adding config "c" =
"ttyUSB0"
2023-10-05 13:09:08.643789 [INFO
                                   1 [
                                                  Port 0: adding config "b" =
"4800"
2023-10-05 13:09:08.643804 [WARNING ] [
                                                  ] Please note that Oregano
Systems' eSync utility is not SyncE - Synchronous Ethernet!
                                                 ] Syn1588Ifc requires at
2023-10-05 13:09:08.643814 [INFO
                                 ] [syn1588
least:
2023-10-05 13:09:08.643819 [INFO
                                   ] [syn1588
                                                  1 - linux driver version 1.4-
15-q05b7283
2023-10-05 13:09:08.643823 [INFO
                                  ] [syn1588
                                                  ] - windows driver version
10/05/2017, 10.9.16.182
2023-10-05 13:09:08.643837 [INFO
                                 ] [syn1588
                                                 ] Device /dev/syncD0 found
2023-10-05 13:09:08.643880 [INFO
                                 ] [syn1588
                                                  ] syn1588(R) PCIe NIC
Revision 2.1, Build 876
2023-10-05 13:09:08.643893 [INFO
                                                  1 Board revision 2.1.2.0
                                  ] [syn1588
                                                  ] Serial Number: 011803176
2023-10-05 13:09:08.643908 [INFO
                                 ] [syn1588
2023-10-05 13:09:08.644035 [INFO
                                  ] [clock
                                                  ] Using Oregano Systems;
syn1588(R) PCIe NIC Revision 2.1; 8C:A5:A1:00:06:95 with ClockId
8c:a5:a1:ff:fe:00:06:95
2023-10-05 13:09:08.968835 [INFO
                                 ] [CeSyncengine ] Using Nmea and PPS for
synchronization
2023-10-05 13:09:09.304562 [WARNING ] [CeSyncengine ] No valid reference time
received!
2023-10-05 13:09:09.721087 [INFO
                                 ] [CeSyncengine ] UTCTime: 110909 UTCDate:
051023
2023-10-05 13:09:09.721134 [INFO ] [CeSyncengine ] Using external
synchronization source with reference time
                                  ] [syn1588
2023-10-05 13:09:11.199930 [ERROR
                                                 ] Syn1588Impl: readReg error:
0 \times 000000040
2023-10-05 13:09:13.811133 [WARNING ] [CeSyncengine ] Wait for external signal
timed out
2023-10-05 13:09:16.000394 [INFO
                                  [CeSyncengine ] UTCTime: 110911 UTCDate:
051023
2023-10-05 13:09:17.000708 [INFO
                                   [CeSyncengine ] UTCTime: 110912 UTCDate:
051023
2023-10-05 13:09:18.000559 [INFO
                                   ] [CeSyncengine ] UTCTime: 110913 UTCDate:
051023
2023-10-05 13:09:19.000870 [INFO
                                   [CeSyncengine] UTCTime: 110914 UTCDate:
051023
2023-10-05 13:09:19.001861 [INFO
                                   ] [CeSyncengine ] UTCTime: 110915 UTCDate:
051023
                                   [CeSyncengine ] UTCTime: 110916 UTCDate:
2023-10-05 13:09:20.001387 [INFO
2023-10-05 13:09:20.001476 [ERROR
                                   ] [syn1588 ] Syn1588Impl: readReg error:
0x00000040
2023-10-05 13:09:20.002415 [INFO
                                   [CeSyncengine ] UTCTime: 110917 UTCDate:
051023
2023-10-05 13:09:21.000699 [INFO
                                   [CeSyncengine ] UTCTime: 110918 UTCDate:
051023
2023-10-05 13:09:22.000706 [INFO
                                   ] [CeSyncengine ] UTCTime: 110919 UTCDate:
051023
```

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After the information header from the eSync utility the synchronization process will deliver also information on the process of synchronization depending on the verbosity level. Below, a typical synchronization process output with verbosity level info is shown.

```
2023-10-05 13:09:17.000708 [INFO
                                    ] [CeSyncengine ] UTCTime: 110912 UTCDate:
051023
2023-10-05 13:09:18.000559 [INFO
                                    ] [CeSyncengine ] UTCTime: 110913 UTCDate:
051023
2023-10-05 13:09:19.000870 [INFO
                                    ] [CeSyncengine ] UTCTime: 110914 UTCDate:
051023
2023-10-05 13:09:19.001861 [INFO
                                    ] [CeSyncengine ] UTCTime: 110915 UTCDate:
051023
2023-10-05 13:09:20.001387 [INFO
                                    ] [CeSyncengine ] UTCTime: 110916 UTCDate:
051023
2023-10-05 13:09:20.002415 [INFO
                                    ] [CeSyncengine ] UTCTime: 110917 UTCDate:
051023
                                    ] [CeSyncengine ] UTCTime: 110918 UTCDate:
2023-10-05 13:09:21.000699 [INFO
051023
2023-10-05 13:09:22.000706 [INFO
                                    ] [CeSyncengine ] UTCTime: 110919 UTCDate:
051023
```

Selecting a GPS Receiver

For connecting a GPS receiver to either a syn1588[®] PCle NIC or a syn1588[®] Dual NIC one requires two connections:

- the 1PPS signal
- the serial NMEA data stream

While the 1PPS signal is connected to any of the available User I/Os (SMA connectors) of the syn1588[®] NIC any standard UART interface of the PC or server – even USB-to-Serial converters or cables will do – can be utilized for connecting the serial line. Basically, almost every GPS receiver provides both a 1 PPS signal as well as a serial NMEA0183 stream (via UART).

Please check the signaling of the 1PPS signal provided by the GPS receiver against the specifications of the syn1588[®] PCle NIC or a syn1588[®] Dual NIC. The syn1588[®] NICs expect a 50 ohm 3V3 signal. Please check the respective datasheet for a full specification of the interface.

Please note, that when connecting a GPS receiver to a syn1588® PCIe NIC one has to operate the syn1588® card in IEEE1588 Master mode. Please further note, that we generally recommend the high-stability OCXO oscillator option for all IEEE1588 Master applications.

Meinberg GPS Solution

If one requires a reliable and accurate solution, Oregano Systems recommends GPS receivers from Meinberg (http://www.meinberg.de). For example the

Meinberg GPS180

(http://www.meinbergglobal.com/english/products/3u-gps-clock-lc-display.htm).



Figure 2 Meinberg GPS180



Figure 3 Meinberg GPS180 (front/rear view basic configuration)

Required Equipment for Meinberg GPS180

Connector: 96-pin VG-female DIN 41612 a+b+c

Ordering @ Digikey: manufacturer: Harting, part number: 09032966845



Figure 4 96-pin VG-female DIN 41612 a+b+c

Pin	Туре
1	VCC in (+5V)
2	VCC in (+12V)
3	
4	PPS out
5	GND
6	PPS in
7	GND
8	TC_DCLS in
9	TC_AM in
10	Reserve 0
11	GND
12	-4.096MHz in
13	+4.096MHz in
14	GND
15	Board_ID0
16	Board_ID1
17	Board_ID2
18	Board_ID3
19	Time Sync in
20	GND
21	10MHz in
22	GND
23	Reserve 1
24	RxD in
25	Slot_ID0
26	Slot_ID1
27	Slot_ID2

28	Slot_ID3
29	+USB
30	-USB
31	GND
32	GND

Table 1Pin assignment GPS180

Attenuator: 3db for 1PPS



Figure 5 Attenuator 3DB 50Ohm SMA

Ordering @ Digikey: Manufacturer: Crystek Corporation, part number: CATTEN-03R0

Cable: USB-A to open end



Figure 6 Cable USB-A to open end

Ordering @ Digikey: Manufacturer: Molex, part number: 0887283200

Test setup with Meinberg GPS180

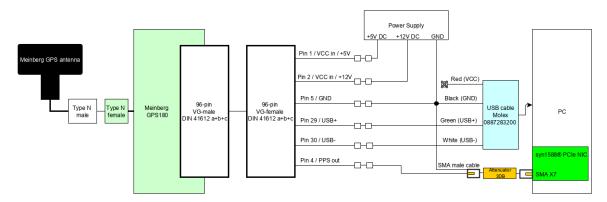


Figure 7 Meinberg Test setup

Navilock GPS Solution

If one requires a simple device for testing, a Navilock receiver (https://www.navilock.com/) is fine as well. For example the

Navilock NL-8004P

(https://www.navilock.com/produkte/G_62527/merkmale.html).



Figure 8 Navilock NL-8004P



Figure 9 Navilock Connector MD6 male

Required Equipment for Navilock NL-8004P

Cable: Navilock 62928



Figure 10 Navilock MD6 female serial> 5 x open wire LVTTL (3.3 V) 52 cm cable

Ordering @ Navilock: part number: 62928

Cable: FTDI TTL-232R-3V3-WE



Figure 11 FTDI TTL-232R-3V3-WE cable

Ordering @ Digikey: Manufacturer: FTDI, part number: TTL-232R-3V3-WE

Cable: SMA male to open end



Figure 12 SMA male cable

Resistor: 10k Ohm



Figure 13 Resistor 1k2 Ohm

Test setup with Navilock NL-8004P

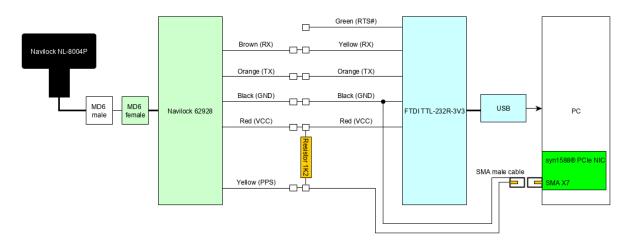


Figure 14 Navilock Test setup

Frequent Issues

• check the serial communication, specially the baud rate. Serial cable connection might require a "null modem adapter" inserted



e.g: Phoenix Contact at Mouser no: 651-2708753

- Configure the GPS receiver output to hold just the required (timing) information. Serial terminal is very slow (typically 4800 baud) which limits the number of characters that can be transferred within a second. GPS receivers might be configured to overwhelm the input buffer.
- Check the level of the 1PPS signal provided by the GPS receiver. The syn1588® NICs expect 3V3 signalling on their inputs.



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