An Introduction to SMPTE 2022 with SMPTE 2059

SMPTE 2059 Use Case

With the rising growth of video transport over IP networks, the demand for remote real-time video production has also increased. In the past, real-time video production needed to be performed on location – using a mobile production studio and local talent.

Today, video can be reliably transported over IP networks in uncompressed, compressed or lightly compressed formats suitable for contribution video streams. The SMPTE (Society of Motion Picture and Television Engineers) 2022 family of standards describes this method of video transport and associated Forward Error Correction (FEC) protocol for IP networks.

IP networks have large latency variations, which require a means of synchronizing and switching between video streams. The IEEE1588 (Precision Time Protocol) allows for precise clock synchronization over Local Area NEtworks (LANs) and Wide Area Networks (WANs). A derivative of this protocol (SMPTE 2059) is used to generate clocks and timestamps for remote video sources, and for those sources to be aligned and edited at a central location.

This paper describes a SMPTE 2059 implementation within SMPTE 2022 end points (specifically SMPTE 2022-5/6), and details a demonstration system developed by Macnica Americas, Oregano Systems, and Altera.

Background

Currently, the standard way of moving video signals between video cameras, displays, and associated equipment is the Serial Digital Interface (SDI) interface. The SDI interface can carry video, audio, and ancillary data. A significant limitation of SDI is that it can only carry data over a short distance. Additionally, SDI can only be switched using dedicated SDI switches.

Transmitting video over IP networks removes the cable length limitations associated with SDI and allows for existing IP network infrastructure to be utilized.

Applicable Standards

The SMPTE 2022 Standard (specifically sections 1, 2, 5 & 6)

The SMPTE 2022 standard describes the transport of real-time video over IP networks, and an associated Forward Error Correction (FEC) scheme designed to guarantee lossless transport over networks with performance parameters compatible with the FEC scheme.

For the purpose of this paper, the focus will be on the SMPTE 2022-5/6 standards (ratified December 2012), commonly referred to as the “high bit rate” or “uncompressed” versions of the standard. The SMPTE 2022-1/2

standards (ratified May 2007) are also defined below for context.

The SMPTE 2022-6 standard describes encapsulating the raw uncompressed SDI stream into Real-time Protocol (RTP) packets, and the RTP packets into User Datagram Protocol (UDP) packets, and Internet Protocol (IP) packets. The RTP protocol includes a timestamp, and the SMPTE 2022-6 standard describes an optional Video Timestamp. The Video Timestamp is a more appropriate timestamp to use for stream synchronization, but since it is an optional field, the RTP timestamp may need to be used.

The SMPTE 2022-5 standard adds Forward Error Correction (FEC) data to the SMPTE 2022-6 packet stream.

The SMPTE 2022-1/2 sections deal with what is often referred to as “low bit rate” or “compressed” versions of the standard.

The SMPTE 2022-2 standard describes the transport of compressed video TSs (TS) over IP networks – similarly to how the SMPTE 2022-6 standard describes the transport of uncompressed video.

The SMPTE 2022-1 standard describes a Forward Error Correction scheme for SMPTE 2022-2, which is similar to SMPTE 2022-5.

The SMPTE 2059 Standard

The SMPTE 2059 standard has not yet been ratified. As of August 2014, the standard is in the “Comment Resolution Phase” within the SMPTE committee. The SMPTE 2059 standard is broken into two sections:

SMPTE 2059-1 defines the SMPTE Epoch (moment in time) as a reference point for all alignment signals. This standard presents formulae for aligning video timing signals to the SMPTE Epoch. It also describes the calculations required to derive the SMPTE alignment signals from the IEEE1588-2008 PTP Data.

SMPTE 2059-2 defines a profile for the IEEE1588-2008 standard. The IEEE1588-2008 standard introduces the concept of a profile, which specifies combinations of options and attributes to support a given application. The SMPTE 2059-2 standard conforms to that definition of an IEEE1588-2008 Profile.

The IEEE1588-2008 Standard

The IEEE1588 standard describes a protocol using timestamp packets that allows remote endpoints to generate synchronized timestamps and precisely aligned timing signals. The IEEE1588-2008 standard is used as a basis for synchronization in SMPTE 2059.

The IEEE1588 standard requires a Grand Master clock and time reference. The IEEE1588 end points all synchronize to this Grand Master clock.

In the context of Video Transport, the WAN needs every media capture device to be an IEEE1588 endpoint synchronized to the Grand Master clock. The termination point in the broadcaster network is also an IEEE1588 end point. This termination point uses the time stamp data in each media stream to align the media streams.

The JPEG 2000 (J2K) Video Compression Standard and associated TS Profile

The most common compression protocol for contribution video is the J2K protocol. The J2K protocol is a frame based compression protocol that can be losslessly re-compressed.

In cases where compressed video transport is required, the compressed video stream is encapsulated by the TS protocol. The ISO/IEC 15444-1 AMD 3 document provides a profile for TS encapsulation of J2K.

Putting it Together- How all of these standards relate

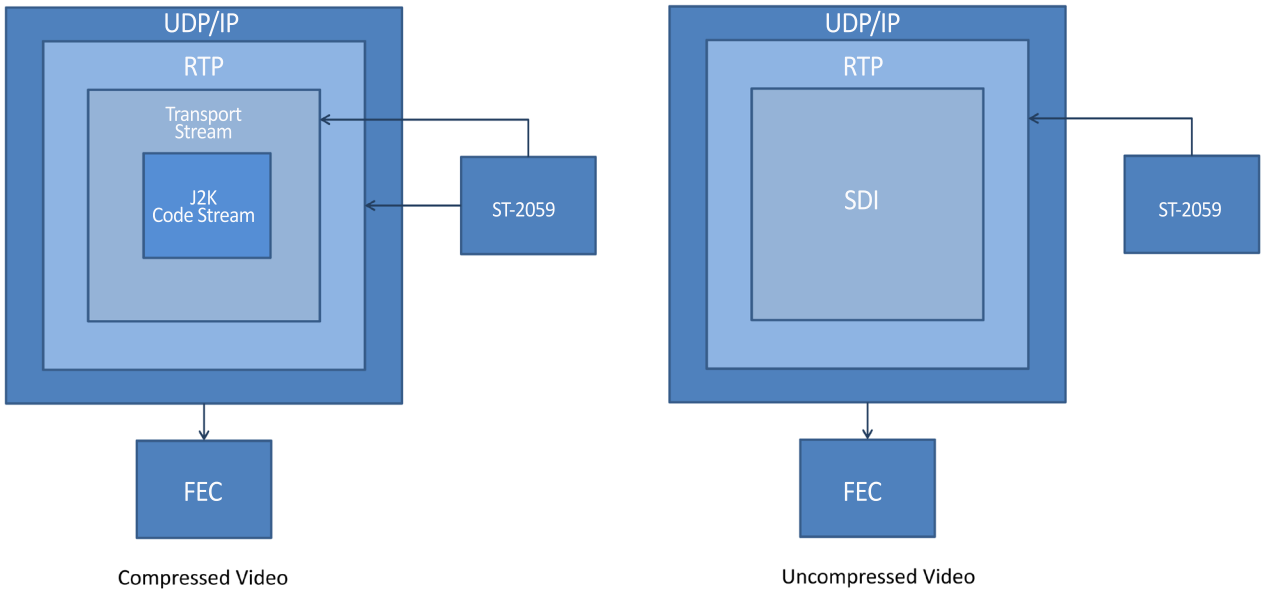

Figure 1: SMPTE 2022 and SMPTE 2059 Protocol Layering

The diagram in Figure 1 shows the protocol layering for compressed and uncompressed video over the respective SMPTE 2022 standards – and J2K TS if applicable.

The SMPTE 2059 standard is implemented as a module at all nodes. It provides timestamps and video synchronization / clocking signals.

The SMPTE 2022 and J2K TS standards require timestamps. In the presence of SMPTE 2059, these timestamps are provided by the SMPTE 2059 module, which generates the timestamps using the IEEE 1588 protocol.

The SMPTE 2022 transmitter inserts the generated timestamps into the RTP and/or media payload headers. If J2K TS is present, the generated timestamps are inserted into the J2K TS.

The SMPTE 2022 receiver uses the generated timestamps with a programmable time offset to align the received streams using the timestamps present in the RTP Header, Media Payload Header, or J2K TS. The SMPTE 2022 receiver also uses synchronization pulses generated by the SMPTE 2059-2 module to generate a recovered SDI clock or other media clock. Streams are frame-aligned (genlocked) using video signals derived from the SMPTE 2059 timestamp relative to the SMPTE 2059 “epoch time.”

While SMPTE 2022 is a common transport protocol for use with SMPTE 2059, SMPTE 2059 may be used in non-SMPTE 2022 transport environments.

When SMPTE 2059 is used in conjunction with compression, while stream alignment and genlock need to occur after decoding.

SMPTE 2022 / SMPTE 2059 Architecture

This architecture example shows an uncompressed SMPTE 2022-5/6 transmitter and receiver integrated with SMPTE 2059.

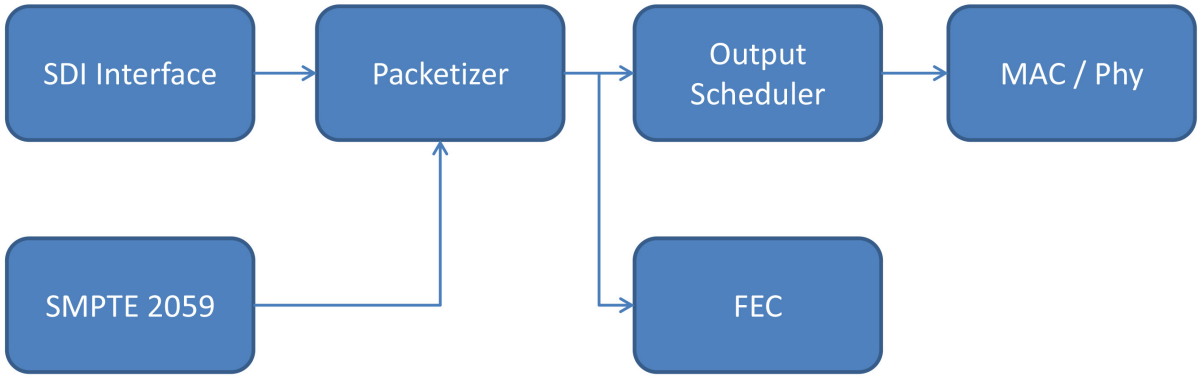

Figure 2: SMPTE 2022-5/6 Transmitter with SMPTE 2059-2

In the transmit path, it is assumed that the SDI input is synchronized to the SMPTE 2059 clock. The SMPTE 2059-2 module generates timestamps. These timestamps are inserted into the media payload packets by the packetizer.

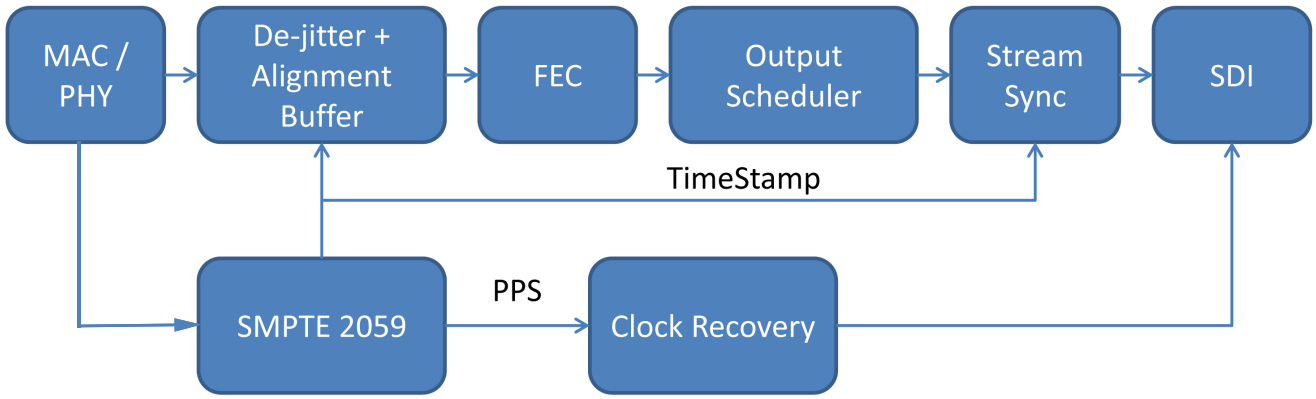

Figure 3: SMPTE 2022-5/6 Receiver with SMPTE 2059-1/2

In the receive path, the SMPTE 2059-2 module is used for timestamp and Pulse Per Second (PPS) generation.

The timestamp plus a latency offset synchronizes the reading of multiple streams from the de-jitter buffer. At that point, the streams are then synchronized down to the packet level. If FEC is used in the system, latency through the FEC system must be accounted for in the per-stream latency calculation. This will packet-align the streams at the egress of the FEC sub-system.

The stream sync module aligns the streams at the media interface level. Output streams are genlocked by this module. The de-jitter and alignment buffers align the streams to within a packet time, such that minimal buffering is required by the stream sync module.

Macnica has a PLL-based clock recovery module that is used in conjunction with the SMPTE 2059-2 module to recover SDI clock from the SMPTE 2059 module PPS signal.

SMPTE 2022-5/6 and SMPTE 2059-2 Demo at IBC 2014

The SMPTE 2022-5/6 and SMPTE 2059-2 demo is the result of collaboration between Macnica Americas, Orega-no Systems, and Altera.

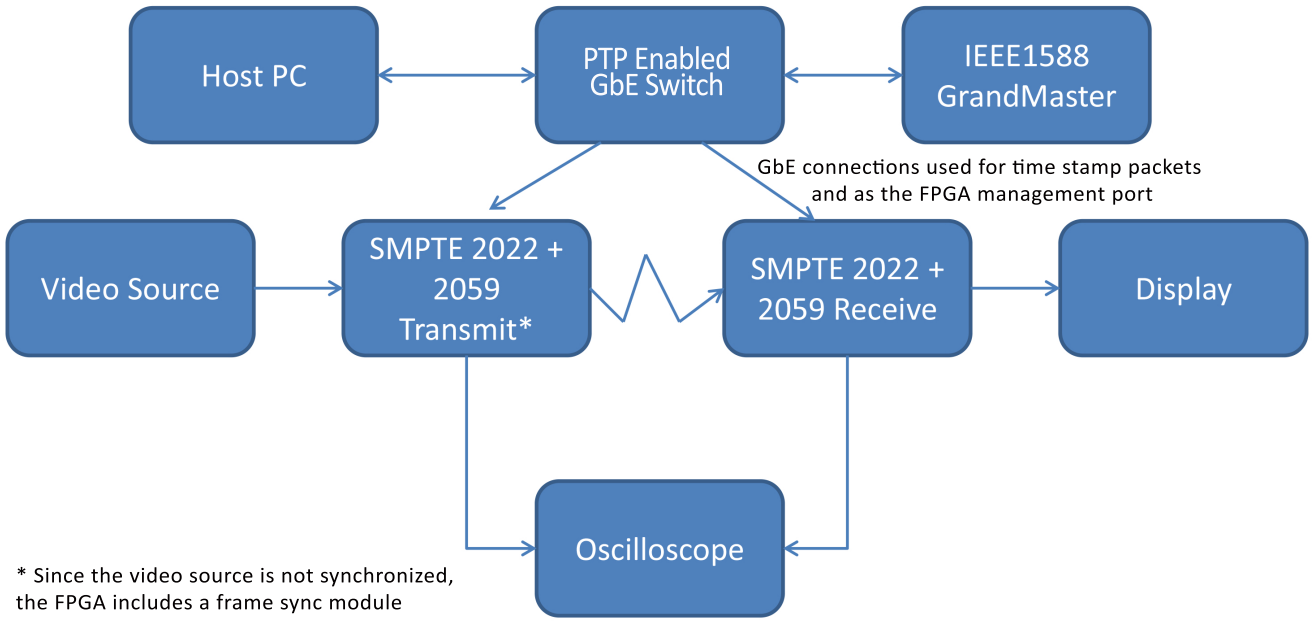

Figure 4: SMPTE 2022 & SMPTE 2059 Demo at IBC 2014

The demo shows the SMPTE 2059-2 Clock Recovery functionality with the transmitter and receiver both generat-ing synchronized clocks using the SMPTE 2059 module. An oscilloscope shows the aligned sync signals or recov-ered clocks.

Since the video source is not using an IEEE 1588 synchronized clock, the SMPTE 2022 transmitter includes a frame buffer to synchronize the video source to the SMPTE 2059 synchronized clock.

Demo Equipment List

- Two Altera Stratix V GX Development Boards
- Two QSFP+ Optical Transponders
- One QSFP+ Octopus Optical Cable
- SDI Video Source
- SDI Video Display (or SDI to HDMI Convertor and HDMI Display)
- Gigabit Ethernet Switch
- IEEE 1588 Grand Master
- Two channel oscilloscope for clock monitoring

IBC 2014 Demo Location

The demo will be available for viewing at Altera's booth (1.F13).

SMPTE 2022 / SMPTE 2059 Development and Integration Timeline

The development is broken into three phases:

Phase 1: IP Integration and generation of synchronized clocks using SMPTE 2059 (complete)

Phase 2: Alignment of streams in time using SMPTE 2059 time stamps

Phase 3: Genlock of streams using SMPTE 2059 time stamps and synchronized clocks

The development timeline is estimated, and heavily dependent on the ratification of the SMPTE 2059 specification.

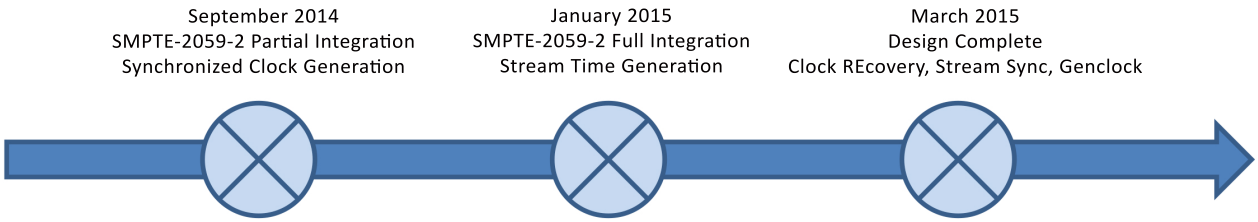

Figure 5: SMPTE 2059 Development Timeline

Macnica Americas Support

Macnica Americas IP Development and Design Services engineers form one team. Each IP sale includes a generous number of support hours. In addition to IP support, additional design services can be included for custom design features and/or IP integration.

Oregano Systems Support

Being an Embedded Systems Design company Oregano Systems offers not only extensive design support for IP core customer but is willing to adapt the both PTP core and the underlying firmware to the specific requirements of a given application.

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