



syn1588® Software Suite

# Release Roadmap

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## 1 Release Schedule

New releases of the Oregano Systems' syn1588® Software Suite are usually scheduled to be published quarterly, by the end of each quarter.

- Q1 – March/April
- Q2 – June/July
- Q3 – September/October
- Q4 – December/January

Oregano Systems reserves the right to change this release schedule for any reason, cancel scheduled releases, or add additional releases as we see fit.

The below plan is not set in stone and we may be able to accommodate your specific requirements. If you are interested in specific features listed below, require some of the features sooner, or have a request for an unlisted feature, contact Oregano Systems (contact@oregano.at or sales@oregano.at).

## 2 Planned Features Q4-2022

### 2.1 Q4/2022 Release

#### 2.1.1 syn1588® technology

- Future-proof Linux module for seamless support of all syn1588 technology applications. One main part of this is the support of complex operations at driver-level and directly connects with the new C-based syn1588 API.
- Finalize the new windows driver for NDIS 6.3 compatible for the syn1588 PCIe Rev 2.3

#### 2.1.2 Basic syn1588® C API

The paradigm for the old syn1588 (and shared memory) API was based on the following points:

- Portability to various bare metal and OS-based systems: the syn1588 technology should be useable and portable to all platforms, bare metal and different OS-based.
- Adaptability: As the syn1588 technology

#### 2.1.3 syn1588® PCIe NIC: new features

- New clocking structure: Analogue frequency adjustment, which increases the achievable accuracy from +/- 8 ns down to +/- 2 ns → this requires the new Linux module and the new PTP clock control implementation
- New clocking structure: Support for Synchronous Ethernet

## 3 Mid-term plans for early 2023

### 3.1 Synchronous Ethernet

Implementation of the ESMC protocol for basic and extended Synchronous Ethernet support.

### 3.2 Extended syn1588 C API

Shift feature support for the syn1588 technology from the current C++ syn1588 API into the new C API or directly into the new Linux and Windows driver were applicable.

### 3.3 New PTP Clock control implementation

### 3.4 PTP v2.1 option support

Add optional IEEE1588-2019 features depending on market/customer demand.

### 3.5 PTP for Power Industry (IEC 61850-9-3:2016)

The target platform for this feature is the syn1588® Dual NIC and the syn1588® redSync utility as this provides the necessary support for this feature set. The implementation can be subdivided into

1. PRP with PTP support
2. HSR with PTP support

The PRP/PTP solution will be the first part to be implemented, whereas the HSR/PTP solution would be implemented later.

The schedule of this implementation depends mostly on customer demand. Demand for PRP/PTP has been shown but we have not seen demand for HSR/PTP.

## 4 Long term plans

The following features are currently on our list but will be implemented on a case-by-case base. I.e., currently these features are not scheduled for a specific release. If the demand for a feature is raised, we can evaluate the roadmap.

### 4.1 Shared memory API 2.0

This is currently put on hold as we are evaluating other means of status/control management (gRPC or similar) of the syn1588® PTP Stack and utilities that may replace or extend the current shared memory in the far future.

### 4.2 PTP Unified Monitoring Model based on YANG

### 4.3 Extension of the redSync utility

- ➔ Using more than two PTP Masters as time source

## 4.4 Support for optional PTP v2.1 Features

4.4.1 Alternate timescale offsets

4.4.2 Path trace

4.4.3 Holdover upgrade

4.4.4 Common mean link delay service

4.4.5 Configurable correction of timestamps

4.4.6 Calculation of delay asymmetry

4.4.7 Grandmaster Cluster

4.4.8 Alternate Master

4.4.9 Unicast Discovery

4.4.10 Layer-1 based synchronization performance enhancement

## 5 PTP Version 2.1 – IEEE1588-2019

This chapter summarizes and collects the different new features for IEEE1588-2019 aka PTP v2.1. The IEEE1588-2019 standard has been officially published on June 16<sup>th</sup> 2020.

The intention of this document is to act

- a.) as an information for externals to inform about the planned implementation as well as their priority
- b.) and as an internal guideline (some sort of development roadmap) for adding the new functions to the syn1588® PTP Stack source code.

A good starting point is chapter 19 of [1] which describes the compatibility of v2.1 with v2.0 and v1.0 of the IEEE1588 standard.

The information in this chapter is based on the status of July 2021.

### 5.1 Overview

The IEEE1588-2019 standard defines new, optional functions listed in the following table. For each feature, its implementation status is given as well as whether Oregano System currently plans to implement it.

Further note, we decided to use priorities for the new functions but not a specific release date. We will add all new functions depending on their priority as soon as possible. They will be made available with our quarterly releases of the syn1588® PTP Stack.

Note, this document is “work-in-progress”. New information or customer requests might change the priority or the implementation of new functions.

If you require a certain PTP v2.1 feature, please contact Oregano Systems so we can add/re-order the feature-list according to the presented business case.

Table 1: PTP v2.1 new, optional features

PTP feature (with IEEE1588-2019 chapter)	Implemented	Focus	Priority (1)
8. (new) PTP datasets	N	Y	1
13. (new or updated) PTP message formats	N	Y	1
16.1 Unicast message negotiation	Y		
16.2 Path trace	N	Y	
16.3 Alternate timescale offsets	N	Y	9
16.4 Holdover upgrade	N	Y	
16.5 Isolation of PTP instances running under profiles specified by different standards organizations	N	Y	
16.6 Common mean link delay service	N	Y	9
16.7 Configurable correction of timestamps	N	Y	6
16.8 Calculation of the <delayAsymmetry> for certain media	N	Y	6
16.9 Mixed Multicast/Unicast Operation	Y		
16.10 Cumulative frequency transfer method for synchronizing clocks	N	N	
16.11 Slave Event Monitoring	N	Y	8
16.12 Enhanced Synchronization Accuracy Metrics	N	N	
16.13 Message Length Extension	N	N	
16.14 PTP integrated security mechanism	Y (immediate)		
17.2 Grandmaster Cluster	N	Y	
17.3 Alternate Master	N	Y	
17.4 Unicast Discovery	N	Y	
17.5 Acceptable master table	Y		
17.6 Mechanism for external configuration of a PTP instance's PTP port state	Y		
17.7 Reduced state sets and use of the <foreignMasterList> feature	N	N	
18. Interactions between PTP Instances in different PTP domains	N	N	

<sup>(1)</sup> High (1) to low (9) priority



## 6 Further Information

You are looking for further information about our syn1588® product line-up? Please contact Oregano Systems support! We will be pleased to provide you all the required information.



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