Version 1.0 – March 2021

Abstract

This application note describes the special considerations when using the four IO signals for input and output functions on a syn1588® Dual NIC.

The syn1588® Dual NIC offers two network interfaces which own their own syn1588® hardware clock function. These two syn1588® hardware clock functions have to share the 4 user I/Os. Additionally all board related components like the jitter cleaner PLL are just available with interface 1.

Useful Documents

- syn1588® User Guide
- syn1588® Dual NIC Datasheet
- Application Note “syn1588®Clock_M IP Core Register Map” (AN001)
- Application Note “Using the frequency and extclk command and the jitter cleaner PLL of a syn1588® PCIe NIC” (AN008).

Basic Procedure

Prior using any of the four user I/O signals one has to assign the I/O signal to the corresponding syn1588® hardware clock functions. This is done by using the IOMATRIX register. There is one IOMATRIX register available for both syn1588® hardware clock functions. They have to we set up in a way that every I/O signal is assigned only to a single interface. If one violates this sequence the assignment for interface 2 will supersede.

Example 1 – generate a digital frequency signal

One would like to generate a digital 8 kHz clock signal and route it to connector X4.

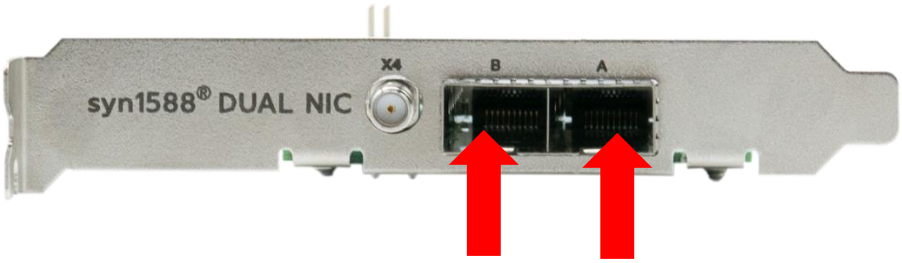

Figure 1: syn1588® Dual NIC - rear view: network interfaces

Since the frequency shall be digitally generated it can be created by the syn1588® hardware clock function #1 and #2. Let's consider we would like to use the syn1588® hardware clock function #2.

This is the command sequence to be issued in the syn1588 utility to output this signal on X4.

```
root@ubuntu:/opt/oregano# ./syn1588
syn1588(R) Driver Interface
Build date: Oct  9 2020 - V 1.12-5 Rev gb411901
Copyright (c) Oregano Systems - Design & Consulting GesmbH 2005-2020
Confidential unpublished data - All rights reserved

Syn1588Ifc requires at least:
- linux driver version 1.4-15-g05b7283
- windows driver version 10/05/2017, 10.9.16.182
Syn1588Impl: Device /dev/syncD0 found
syn1588(R) Hardware Clock M 2.3.5 f=125000000 Hz
Syn1588Impl: Device /dev/syncD1 found
syn1588(R) Hardware Clock M 2.3.5 f=125000000 Hz
Selected syn1588(R) card 0
>listcards
card 0 is 8c:a5:a1:ff:fe:00:09:40
card 1 is 8c:a5:a1:ff:fe:00:09:41
```

The syn1588 utility shows two cards, i.e. a syn1588® Dual NIC. Since we want to assign X4 solely to interface 2 we have to disable it for interface 1.

For this we select interface 1 (card 0), read the IOMATRIX register (0x200), modify the entry for X4 (lowest nibble) to disable any output (write 0x0) and write the value back. For a detailed description of the IOMATRIX register and its function please check the syn1588® User Guide or the AN001 "syn1588®Clock_M IP Core Register Map".

```
>card 0
Selected syn1588(R) card 0
>0x200
0x00430059
>0x200 0x00430050
>0x200
0x00430050
```

Now switch to interface 2 and issue the frequency command.

```
>card 1
Selected syn1588(R) card 1
>frequency d 4 0 8k
Match found for desired frequency: 8000.000000!
Generated frequency will be: 8000.000000 Hz
Waiting 9 seconds for FPGA output to settle
d 4 0 8k
>0x200
0x00430055
```

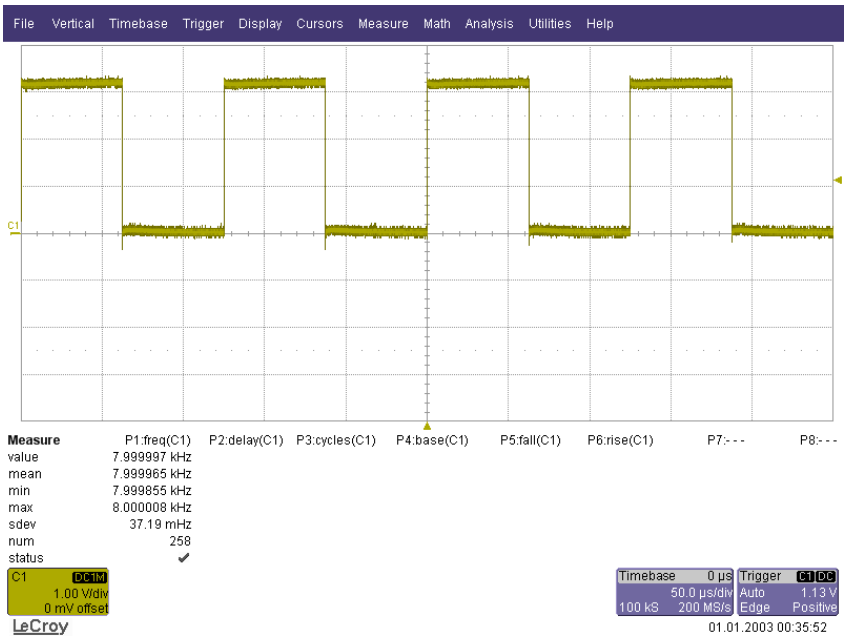

Figure 2 digital 8 kHz clock signal generated on connector X4

Example 2 – generate a PLL frequency signal

One would like to generate a digital 30.72 MHz clock signal and route it to connector X4. Since the frequency has to be generated by the on-board jitter cleaner PLL it has to be created by the syn1588® hardware clock function #1.

This is the command sequence to be issued in the syn1588 utility to output this signal on X4.

```
root@ubuntu:/opt/oregano# ./syn1588
syn1588(R) Driver Interface
Build date: Oct  9 2020 - V 1.12-5 Rev gb411901
Copyright (c) Oregano Systems - Design & Consulting GesmbH 2005-2020
Confidential unpublished data - All rights reserved

Syn1588Ifc requires at least:
- linux driver version 1.4-15-g05b7283
- windows driver version 10/05/2017, 10.9.16.182
Syn1588Impl: Device /dev/syncD0 found
syn1588(R) Hardware Clock M 2.3.5 f=125000000 Hz
Syn1588Impl: Device /dev/syncD1 found
syn1588(R) Hardware Clock M 2.3.5 f=125000000 Hz
Selected syn1588(R) card 0
>listcards
card 0 is 8c:a5:a1:ff:fe:00:09:40
card 1 is 8c:a5:a1:ff:fe:00:09:41
```

The syn1588 utility shows again two cards, i.e. a syn1588® Dual NIC. Since we want to assign X4 solely to interface 1 we have to disable it for interface 2. For this we select interface 2 (card 1), read the IOMATRIX register (0x200), modify the entry for X4 (lowest nibble) to disable any output (write 0x0) and write the value back. For a detailed description of the IOMATRIX register and its function please check again the syn1588® User Guide or the AN001 “syn1588®Clock_M IP Core Register Map”.

```
>card 1
Selected syn1588(R) card 1
>0x200
0x00430059
>0x200 0x00430050
>0x200
0x00430050
```

Now switch to interface 1 and issue the frequency command.

```
>card 0
Selected syn1588(R) card 0
>frequency p 4 1 30720k
Configure jitter-cleaner PLL
This can take several minutes!
Waiting 9 seconds for FPGA output to settle
Wait for the external PLL to lock (max 600 sec.):
600....595....590....585....580..
PLL locked
p 4 1 30720k
>0x200
0x0043005D
```

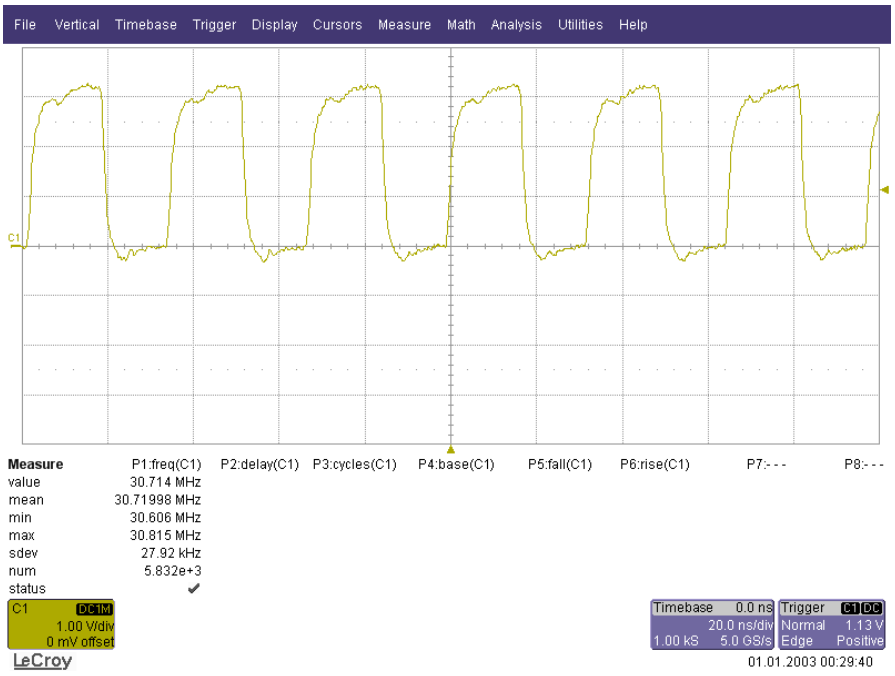

Figure 3 30.72 MHz clock signal generated on connector X4

Literature

AN001. (Version 1.48 - October 2019). *Application Note: "syn1588® Clock M IP Core Register Map".* Oregano Systems.

AN002. (Version 2.8 - March 2019). *Application Note: "Ordering syn1588® PCIe NIC Revsion 2.1".* Oregano Systems.

AN004. (Version 1.6 - May 2019). *Application Note: "syn1588® PCIe NIC - Quick Start Guide".* Oregano Systems.

AN014. (Version 1.5 - April 2019). *Application Note: "syn1588® NIC Updater".* Oregano Systems.

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Oregano Systems
A Meinberg Company

Franzosengraben 8
A-1030 Vienna
Austria
http://oregano.at
contact@oregano.at