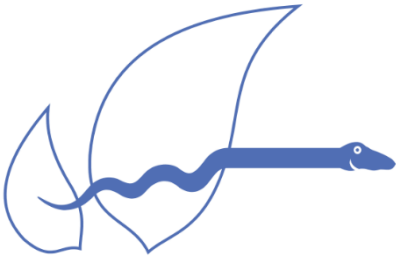

syn1588® Software Suite

Release Roadmap

Version 1.13.2 – July 27th 2021

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0.1 Legals

0.2 Contents

1 Release Schedule

New releases of the Oregano Systems' syn1588® Software Suite are usually scheduled to be published quarterly, by the end of each quarter.

- Q1 – March/April
- Q2 – June/July
- Q3 – September/October
- Q4 - December

Oregano Systems reserves the right to change this release schedule for any reason, cancel scheduled releases, or add additional releases as we see fit.

The below plan is not set in stone and we may be able to accommodate your specific requirements. If you are interested in specific features listed below, require some of the features sooner, or have a request for an unlisted feature, contact Oregano Systems (contact@oregano.at or sales@oregano.at).

2 Planned Features 2021

2.1 Q3/2021 Release

2.1.1 Broadcast Industry: Audio, SDI and SDI LTC signal generation

The Video extension board for the syn1588® PCIe NIC already provides synchronization capability to external Video source signals as well as the generation of basic SDI Video signals (H/F Sync, etc.) for various Video modes.

In addition to these signals, a new hardware supported generation of Audio Alignment Point, SDI Alignment Point and SDI LTC Timecodeword according to SMPTE 2059-1 and 2059-2 is currently scheduled for release with Q3/2021 v1.14.

2.1.2 PTP v2.1 support

Elevate IEEE1588-2019 support from beta to full release.

2.1.3 syn1588 PTP Clock architecture overhaul

We are currently (release Q2/2021 v1.13) running internal tests of a new clock controlling mechanism that utilizes the seasoned algorithms and filters and provides an improved and extensible architecture.
This clock architecture overhaul is scheduled for the next release and already shows a significant improvement in stability and accuracy.

2.1.4 syn1588® Dual NIC: improved support

2.1.5 syn1588® PCIe NIC: new features

- Upgrade the windows driver to NDIS 6.3.

2.1.6 Linux PHC interface for syn1588® hardware

This extension to the Linux syn1588® PCIe and Dual NIC driver allows a standardized access to the base syn1588® hardware clock functionality. Features of the syn1588 hardware, not covered by the Linux PHC interface, are still available via the syn1588 API.

2.1.7 syn1588 API 2.0

This rework will provide improved access to the feature set of the syn1588® hardware.

Note that this will replace the current syn1588 API over the next release cycles, we will provide extensive documentation to make the switch as seamless as possible. You will receive the new API over the next release cycles together with the old API. The current syn1588® hardware

features will still be available via the old syn1588 API during this switchover. New features will only be available via the syn1588 API 2.0.

3 Mid-term plans for 2021

3.1 PTP v2.1 support

Add optional IEEE1588-2019 features depending on market/customer demand.

3.2 PTP Security: Key Exchange

3.3 syn1588® Dual NIC: extended syn1588 API support

3.4 Shared memory API 2.0

This rework will provide improved access to the feature set of the syn1588® software.

Note that this will replace the current shared memory API over the next release cycles, we will provide extensive documentation to make the switch as seamless as possible. You will receive the new API over the next release cycles together with the old API. The current syn1588® software features will still be available via the old shared memory API during this switchover. New features will only be available via the shared memory API 2.0.

4 Long term plans

The following features are currently on our list but will be implemented on a case-by-case base. I.e., currently these features are not scheduled for a specific release. If the demand for a feature is raised, we can evaluate the roadmap.

4.1 PTP Unified Monitoring Model based on YANG

4.2 Extension of the redSync utility

- ➔ Using more than two PTP Masters as time source
- ➔ Utilizing the syn1588® Dual NIC

4.3 Support for optional PTP v2.1 Features

4.3.1 Alternate timescale offsets

4.3.2 Path trace

4.3.3 Holdover upgrade

4.3.4 Common mean link delay service

4.3.5 Configurable correction of timestamps

4.3.6 Calculation of delay asymmetry

4.3.7 Mixed Multicast/Unicast Operation

4.3.8 Grandmaster Cluster

4.3.9 Alternate Master

4.3.10 Unicast Discovery

4.3.11 Layer-1 based synchronization performance enhancement

5 PTP Version 2.1 – IEEE1588-2019

This chapter summarizes and collects the different new features for IEEE1588-2019 aka PTP v2.1. The IEEE1588-2019 standard has been officially published on June 16th 2020.

The intention of this document is to act

a.) as an information for externals to inform about the planned implementation as well as their priority
b.) and as an internal guideline (some sort of development roadmap) for adding the new functions to the syn1588® PTP Stack source code.

A good starting point is chapter 19 of [1] which describes the compatibility of v2.1 with v2.0 and v1.0 of the IEEE1588 standard.

The information in this chapter is based on the status of July 2021.

5.1 Overview

The IEEE1588-2019 standard defines new, optional functions listed in the following table. For each feature, its implementation status is given as well as whether Oregano System currently plans to implement it.

Further note, we decided to use priorities for the new functions but not a specific release date. We will add all new functions depending on their priority as soon as possible. They will be made available with our quarterly releases of the syn1588® PTP Stack.

Note, this document is “work-in-progress”. New information or customer requests might change the priority or the implementation of new functions.

If you require a certain PTP v2.1 feature, please contact Oregano Systems so we can add/re-order the feature-list according to the presented business case.

Table 1: PTP v2.1 new, optional features

PTP feature (with IEEE1588-2019 chapter)	Implemented	Focus	Priority (1)
8. (new) PTP datasets	N	Y	1
13. (new or updated) PTP message formats	N	Y	1
16.1 Unicast message negotiation	Y		
16.2 Path trace	N	Y	
16.3 Alternate timescale offsets	N	Y	9
16.4 Holdover upgrade	N	Y	
16.5 Isolation of PTP instances running under profiles specified by different standards organizations	N	Y	
16.6 Common mean link delay service	N	Y	9
16.7 Configurable correction of timestamps	N	Y	6
16.8 Calculation of the <delayAsymmetry> for certain media	N	Y	6
16.9 Mixed Multicast/Unicast Operation	Y		
16.10 Cumulative frequency transfer method for synchronizing clocks	N	N	
16.11 Slave Event Monitoring	N	Y	8
16.12 Enhanced Synchronization Accuracy Metrics	N	N	
16.13 Message Length Extension	N	N	
16.14 PTP integrated security mechanism	Y (immediate)		
17.2 Grandmaster Cluster	N	Y	
17.3 Alternate Master	N	Y	
17.4 Unicast Discovery	N	Y	
17.5 Acceptable master table	Y		
17.6 Mechanism for external configuration of a PTP instance's PTP port state	Y		
17.7 Reduced state sets and use of the <foreignMasterList> feature	N	N	
18. Interactions between PTP Instances in different PTP domains	N	N	

(1) High (1) to low (9) priority

6 Further Information

You are looking for further information about our syn1588® product line-up? Please contact Oregano Systems support! We will be pleased to provide you all the required information.

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