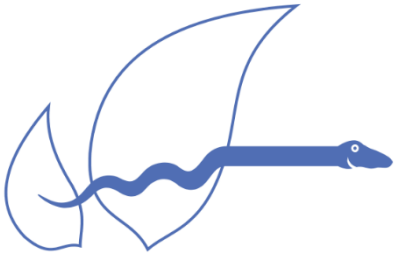

syn1588 ®

PCI Express Ethernet Network Interface Card – Revision 2.3

# syn1588® PCIe NIC

## Data Sheet

**Version 5.2 – September 18th 2023**


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## 0.1 Contents

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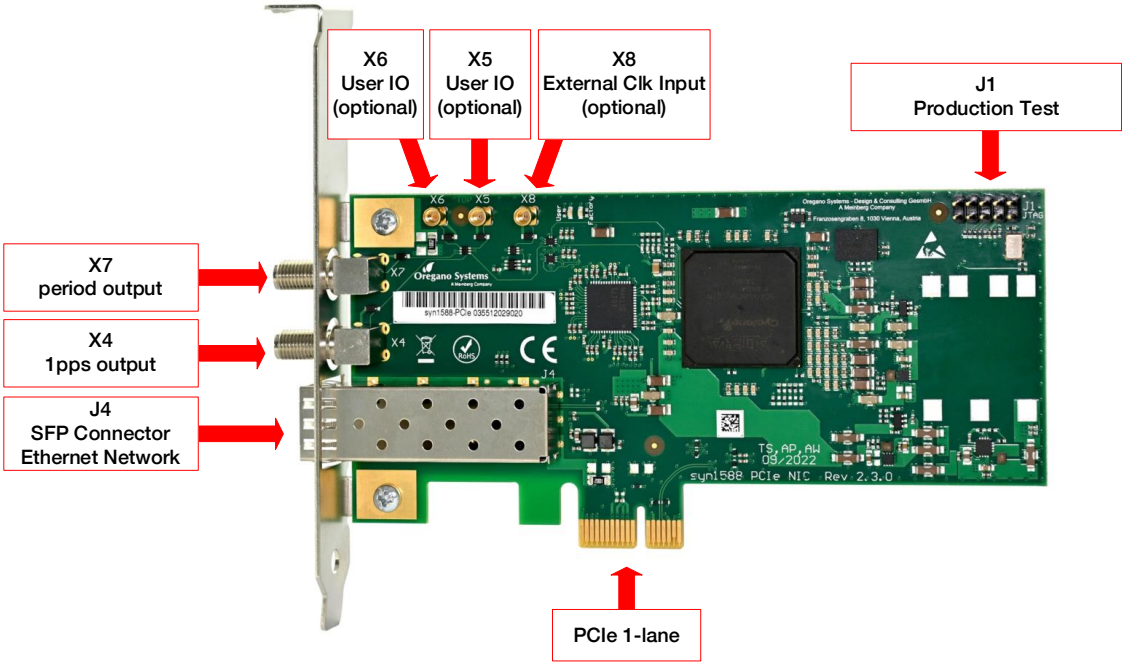




## 0.3 List of Tables

# 1 Overview

## 1.1 Functional description

The syn1588® PCIe NIC is a 100/1000 Mbit Ethernet network interface card (1-lane PCI Express low-profile card) with enhancements to provide the network node with accurate clock synchronization via Ethernet following the IEEE1588 standard.

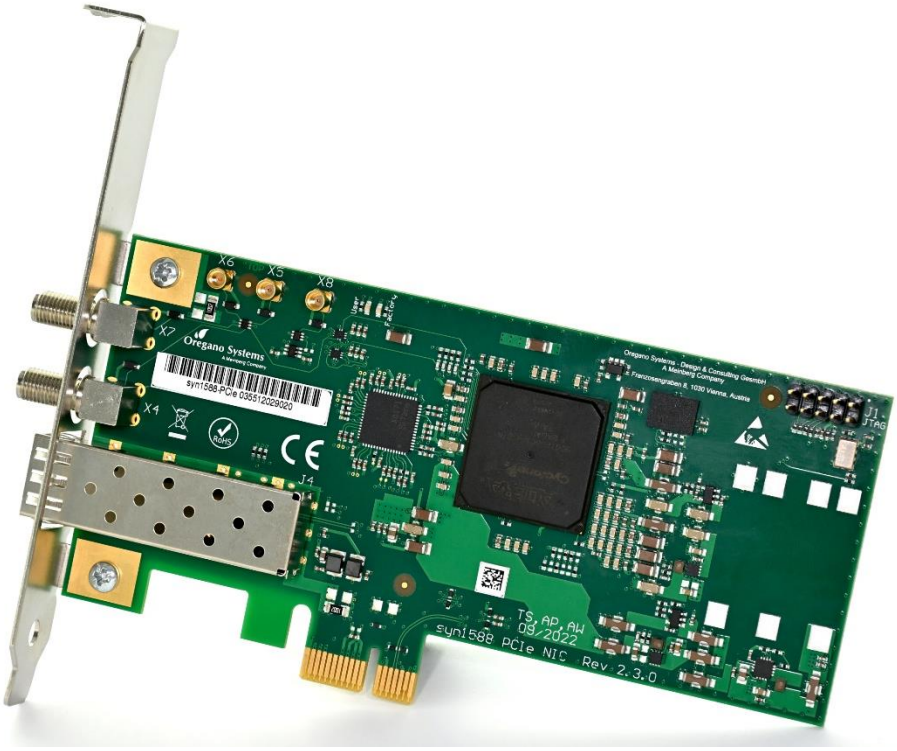


**Figure 1: syn1588® PCIe NIC – Revision 2.3**

The syn1588® PCIe NIC is using the Oregano Systems syn1588® technology for time stamping of arbitrary network packets. The timestamping unit is fully user configurable enabling any type of packet timing application. The syn1588® PCIe NIC provides full support for IEEE1588-2002 as well as IEEE1588-2008 specific features like the patented on-the-fly timestamping mechanism (one-step mode).

The revision 2.3 of the card had been re-designed to optimize for sourcing the electronic components as the whole industry is faced with excessive lead time and unexpected or short-term obsolescence of components. E.g. there is now just a SFP type network interfaces available which also allows using copper based transceiver modules. A new on-board jitter cleaner PLL from SiTime is used now which further improves the accuracy together with the new local oscillators (both TCXO and OCXO).

# 2 Features

The following features are based on the hardware build ID 25 of the syn1588® PCIe NIC – Revision 2.3. Other build versions of the syn1588® PCIe NIC will offer somewhat different capabilities. Please contact Oregano Systems support for details.

## 2.1 NIC Features

- Standard 100/1000 Mbps Ethernet network card following IEEE802.3-2005
- 1-lane PCI Express (PCIe) low-profile card
- Compliant to PCI Express version 2.0 (5 Gbit/s)
  - Compatible with PCI Express version 1.1 (2.5 Gbit/s)
- SFP type network interface
  - Supporting 100/1000 Mbit full-duplex operation for copper SFP transceiver modules
  - Supporting 100 Mbit half-duplex mode[1]
  - Supporting 1000BASE-X for fiber SFP transceiver modules
- 16 kbyte Ethernet transmit FIFO buffer, 64 kbyte Ethernet receive FIFO buffer
- VLAN and IPv6 support
- Promiscuous mode supported
- Driver software available for Linux and Windows. Both 32 bit and 64 bit systems are supported.

[1] Limited cable length (collision detection) for half-duplex mode due to 1-step timestamp insertion logic

## 2.2 IEEE1588 Features[2]

- Fully IEEE1588-2002, IEEE1588-2008 and IEEE1588-2019 compliant
- Support for Oregano Systems' patented syn1588® technology:
- On-the-fly timestamping while sending or receiving time sync packets (1-step mode)
- IEEE1588 hardware clock - the IEEE1588 clock is fully maintained in hardware
- Clock servo operation is controlled by the software without real-time requirements
- IEEE1588 hardware clock utilizes IEEE1588 time format
- Software does not need to execute time format conversion
- syn1588® clock frequency is 125 MHz
- All real-time functions for IEEE1588 are implemented in hardware eliminating real-time constraints for the syn1588® PTP Stack
- IEEE1588 master and slave operation supported[3]
- High quality TCXO oscillator
    - Initial tolerance: 1ppm or better
    - Holdover performance: 0.28 ppm for 24h
- Optional high-stability OCXO oscillator
    - Initial tolerance: 0.5ppm
    - Holdover performance: Stratum 3E compliant
- Up to four programmable input/output signals available on SMA connectors
    - 50 Ω, 3V3 LVCMOS signalling
- 1PPS input and/or output[4]
- Up to two EVENT inputs
- Up to two TRIGGER outputs
- Up to two+two[5] PERIOD outputs
- Optional clock input to drive the syn1588® clock for selected clock frequencies
- Programmable interrupt conditions
- IRIG-B007 output data stream generation
  (DCLS signal, no carrier, BCD + BCD_Year + SBS)
- Optional IRIG-B007 input decoding
  (DCLS signal, no carrier, BCD + BCD_Year)
- On-board jitter cleaner PLL for generating accurate, synchronized single-ended frequencies up to 156.25 MHz

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[2] Requires the Oregano Systems syn1588® PTP Stack to run the protocol engine.

[3] Oregano Systems generally recommends using the high-stability OCXO option for all master applications.

[4] Constant delay of three clock periods to the external output signal. Minimum pulse width is 100 µs.

[5] Beside the two standard PERIOD functions there are two PERIOD light functions available

- Connectivity to an external GPS receiver via the 1 PPS input as well as a serial port of the host PC for external synchronization
  - Serial port not included in the syn1588® PCIe NIC
  - NMEA-0183 RMC messages required
- Binary run-time license for syn1588® PTP Stack included
- Several utilities are available for accessing registers, synchronizing the node's system clock, or synchronizing to an external GPS receiver.
- Software APIs are available allowing the user to write custom software including interrupt service routines accessing the syn1588® functions, accessing all hardware clock related functions and controlling/observing the syn1588® PTP Stack
- syn1588® Linux Live System for fast testing of the syn1588® PCIe NIC without the need of software installation. Just install the syn1588® PCIe NIC in your node and boot the PC using the syn1588® Linux Live System

### 2.2.1 Timestamping

- Programmable timestamping unit on Ethernet receive and transmit path for time stamping IEEE1588 packets
- Independent timestamp FIFOs for Ethernet receive path (256 words) and Ethernet transmit path (16 words) allows timestamping of multiple dense packets without losing data thus removing the software real-time requirements
- Patented on-the-fly timestamping for 1-step operation on Ethernet transmit path
- 1-step timestamping just supported for 100 Mbit and 1000 Mbit full duplex operation
- Timestamping supported for VLAN as well as IPv6 operation
- Timestamping of two external input signals – EVENT: On the rising edge of these external signals a timestamp will be drawn
- For EVENT0 input a 16-entry timestamp FIFO is implemented allowing timestamping of dense events with a distance of just 100 ns
- Extremely high timestamp resolution of 4 ns

### 2.2.2 User Programmable Events

- TRIGGER: Two user programmable single event output signals may be generated
- These TRIGGER signals change their respective state at a programmable time that is derived from the highly accuracy IEEE1588 hardware clock
- TRIGGER0 output is controlled by a 16-entry FIFO providing support for dense event sequences without imposing real-time requirements on the software
- Resolution of all TRIGGER events is +/-4 ns
- Maximum TRIGGER event duration is 32 bit seconds
- PERIOD: Two user programmable periodical output signals may be generated that are derived from the highly accuracy IEEE1588 hardware clock
- The frequency may be selected in the range of mHz to 156.25 MHz
- The resolution of all PERIOD events is $2^{-16}$ ns, i.e. 0,0153 ps
- The maximum PERIOD duration is 65535 seconds (16 bit)

## 2.3 Hardware Options

- High-stability OCXO for master operations or high accuracy applications.
- External clock input for the PTP hardware clock

# 3 Block Diagram

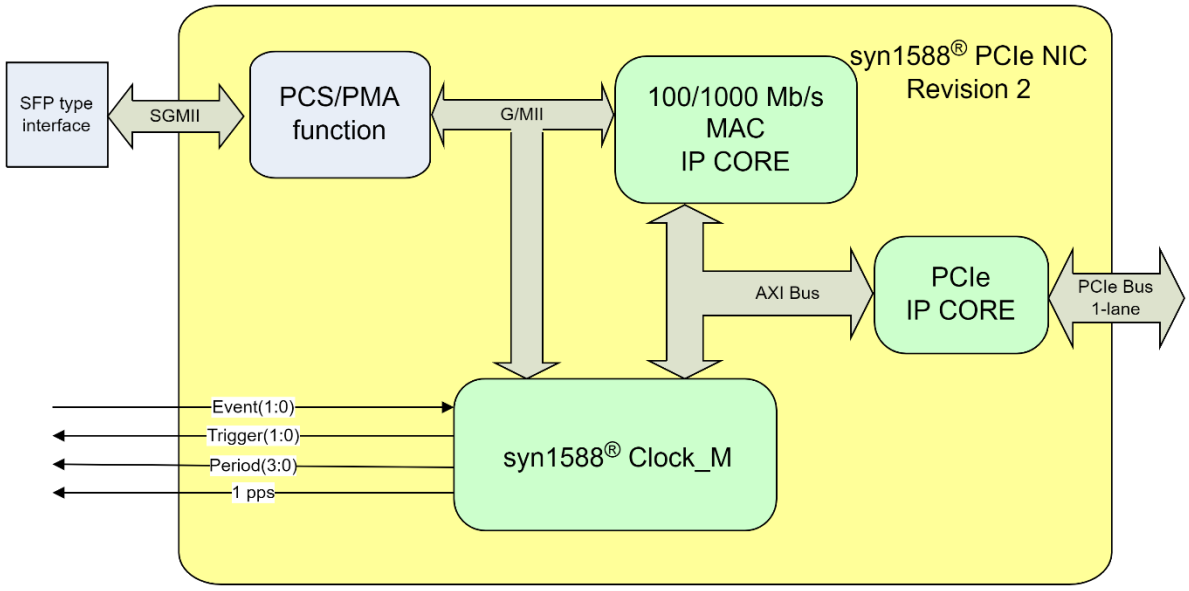


**Figure 2: syn1588® PCIe NIC: block diagram**

The syn1588® PCIe NIC basically consists of a single FPGA containing the following IP cores:

- 100/1000 Mbps Ethernet Media Access Controller (MAC)
- syn1588® Clock_M IP Core
- PCIe interface
- PCS/PMA function

# 4 Mechanics

The following figure shows the dimensions of the syn1588® PCIe NIC board revision 2.3.

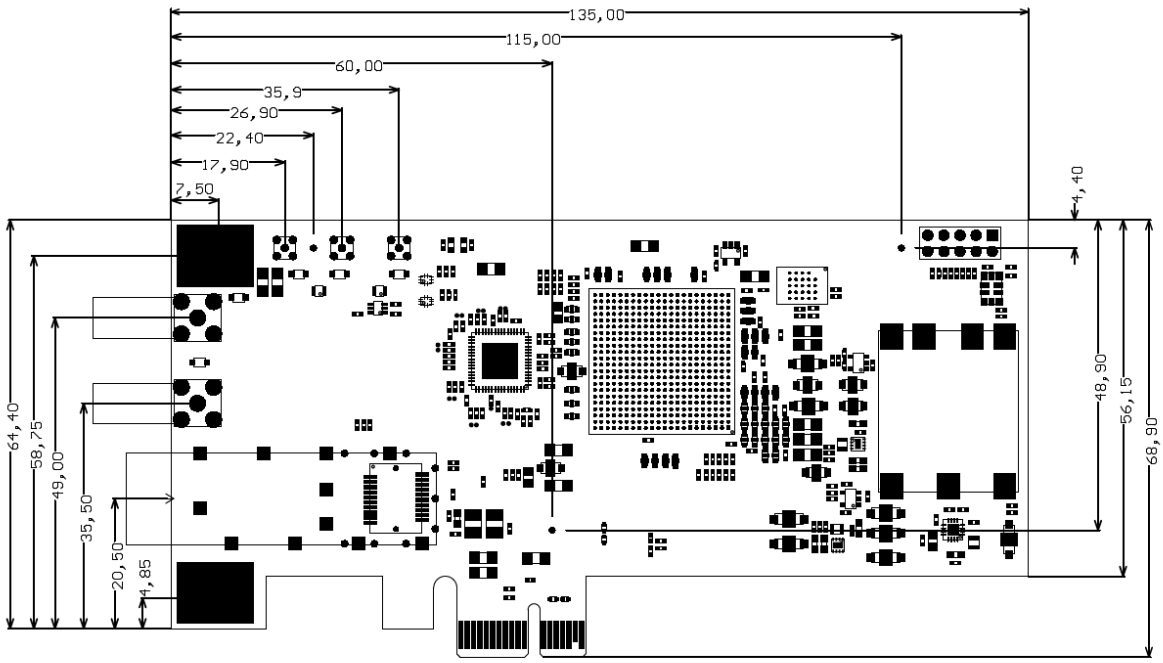


**Figure 3: syn1588® PCIe NIC Revision 2.3: dimensions & placement of connectors (all dimensions are in mm)**

Please note that the position of the connectors at the PCIe bracket did not change with respect to the previous revision 2.0/2.1 of the syn1588® PCIe NIC.

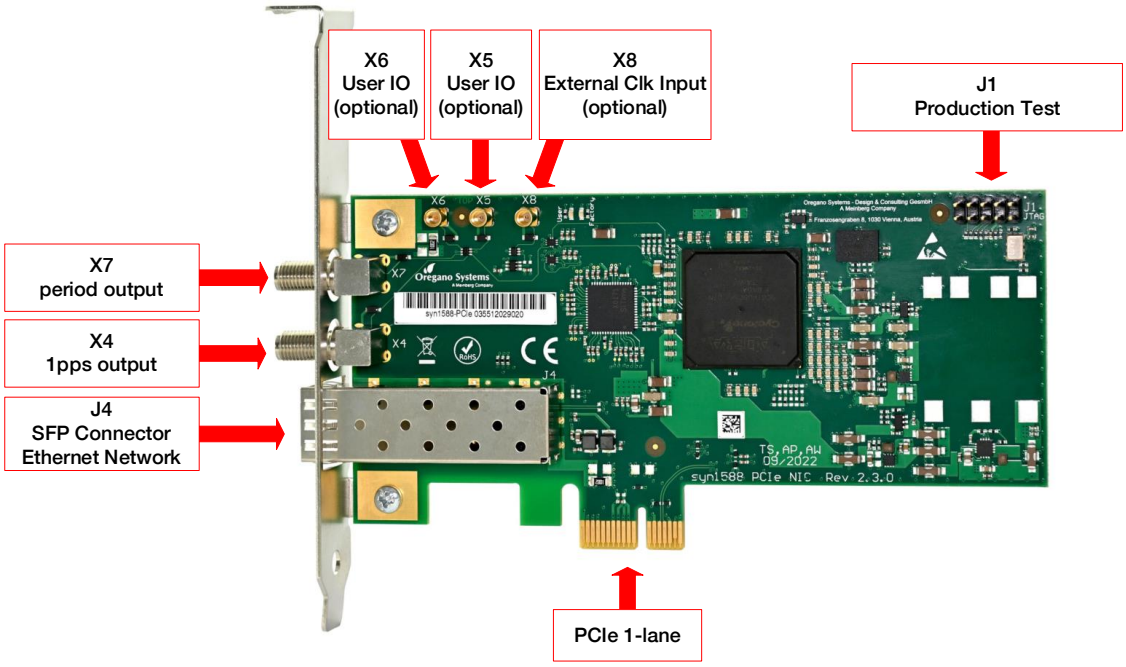


**Figure 4: syn1588® PCIe NIC Revision 2.3: connectors**

Oregano Systems offers two different types of brackets for the syn1588® PCIe NIC to facilitate any type of mounting situation; the card comes with both brackets.

- Low-profile bracket with 2 SMA connectors (default option, mounted)
- Standard bracket with 2 SMA connectors

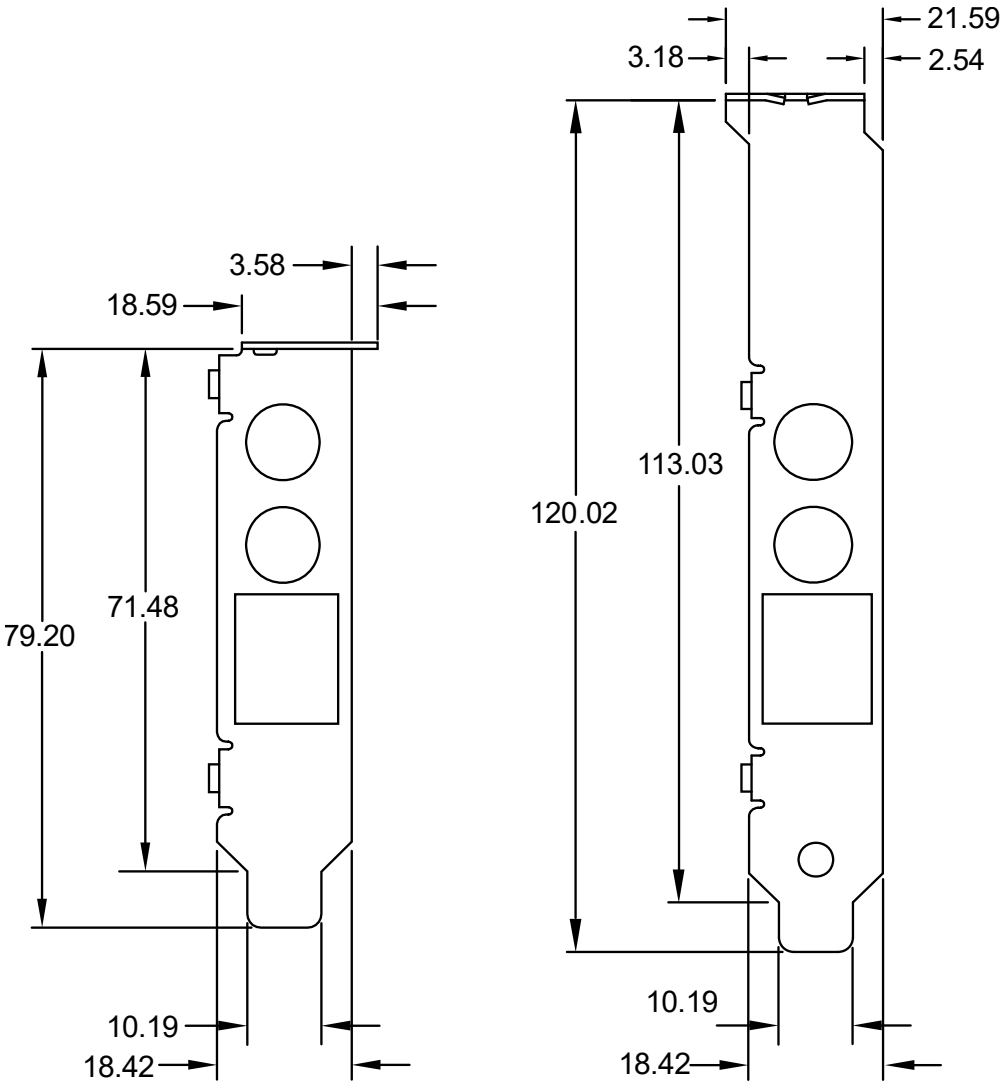


**Figure 5: PCI bracket options**

# 5 Electrical Interface Specification

## 5.1 ESD

All user accessible connectors of the syn1588® PCIe NIC are protected against ESD damage following IEC61000-4-2 15 kV air 8 kV contact.

## 5.2 Power Supply

The syn1588® PCIe NIC revision 2.3 board is operated using the 3V3 power supplied by the PCI Express edge connector. The oscillators – the TCXO as well as the optional OCXO - are powered by highly stable on-board supply which uses the 12V supplied by the PCI Express edge connector.

| DC Characteristics | |
|---|---|
| Minimum DC 3V3 input voltage | 3.0 V |
| Maximum DC 3V3 input voltage | 3.6 V |
| Maximum DC supply current @ 3,3 V | 1.0 A |
| Minimum DC 12V input voltage | 11.5 V |
| Maximum DC 12V input voltage | 12.5 V |
| Maximum DC supply current @ 12V | 0.2 A |

**Table 1 Power supply DC characteristics**

## 5.3 SFP Ethernet Interface (J4)

The SFP interface supports just 1000BASE-X mode using the following SFP transceiver modules.

| Vendor | Type | Mode | Range | Connector | Order Number |
|---|---|---|---|---|---|
| Avago | fiber | 1000BASE-X | short (550 m) | LC | AFBR-5710PZ |
| Avago | fiber | 1000BASE-X | long (10 km) | LC | AFCT-5710PZ |
| Fiberstore | fiber | 1000BASE-X | short (550 m) | LC | SFP1G-SX-85 |
| Fiberstore | fiber | 1000BASE-X | long (10 km) | LC | SFP1G-LX-31 |
| Finisar | fiber | 1000BASE-X | long (10 km) | LC | FTLF1318 |
| Fiberland | fiber | 1000BASE-X | short (550 m) | LC | FLD-SG-MMD-1 |
| Fiberland | fiber | 1000BASE-X | long (10 km) | LC | FLD-SG-SMD-10 |
| Fiberland | copper | 1000BASE-T | 100 m | RJ45 | FLD-SASG-T |

**Table 2 Supported SFP transceiver modules**

All fiber SFP transceiver modules use the LC connector. Using the SR module (850nm) one typically achieves at least 300 m connection distance using a 62.5/125m MMF. Using the LR module (1310nm) one achieves 10 km connection distance using a 9/125m SMF.

## 5.4 User Interface (X4, X5, X6, X7)

There are four connectors available for the user: two SMA at the PCI bracket and two MMCX connectors on board. The function and direction for every of the four connectors is configurable by the user during run-time using the syn1588® Software Suite.

The default configuration of these user IOs is as follows:

- X4: 1 PPS
- X7: period_0 output signal
- X6: event_0 input signal
- X5: disabled

The output signals deliver a standard 3V3 level 50 Ω output signal driving a maximum of 20 mA. The input signals expect a standard 3V3 level signal. The output signals may drive two or three standard loads when using correct 50 Ω cabling.

Two SMA connectors (X4 and X7) are directly available at the PCI bracket while two more connectors (X5 and X6) are available internally. Upon request (via the appropriate ordering code) Oregano Systems supplies the cable to directly connect to a SMA port.

### 5.4.1 SMA Output Characteristics

| | |
|---|---|
| **Output coupling** | DC |
| **Output threshold high** | 2.8 V min |
| **Output threshold low** | 0.4 V max |
| **Absolute maximum applied voltage** | -0 V to 3.465 V |
| **Output to output skew, synchronous** | < 1 ns typical |
| **Output current** | ±20 mA max |

**Table 3 SMA Output Characteristics**

### 5.4.2 SMA Input Characteristics

| | |
|---|---|
| **Input impedance** | 50 Ω nominal |
| **Input coupling** | DC |
| **Voltage level** | 0 to 3.3 V |
| **Absolute maximum input voltage** | -0.5 V to 4.25 V |
| **Minimum pulse width** | 500 ns |
| **Input threshold high** | 2.0 V |
| **Input threshold low** | 0.8 V |

**Table 4 SMA Input Characteristics**

## 5.5 External clock Input Interface (X8)

Optionally there is an external clock input available to allow direct driving the syn1588® hardware clock from this external signal.

| | |
|---|---|
| **Input impedance** | 50 Ω nominal |
| **Input coupling** | DC |
| **Voltage level** | 0 to 3.3 V |
| **Absolute maximum input voltage** | -0.5 V to 4.25 V |
| **Input threshold high** | 2.0 V |
| **Input threshold low** | 0.8 V |

**Table 5 External Clock Input Characteristics**

The ExtClk input is a digital input and thus cannot accept sinewave signals etc. A duty cycle of 30-70 % is required.

## 5.6 Production Test (J1)

The production test connector must be left unconnected while the syn1588® PCIe NIC is operated. Note that there is no special ESD protection for this interface.

# 6 Environmental

## 6.1 Temperature

Operating temperature range 0° C ... +50° C

Storage temperature range -40° C ... +85° C

## 6.2 Humidity

Operating humidity 5% to 80% RH, non-condensing

## 6.3 Weight

Total weight approx. 70 g (without OCXO)

Total weight approx. 75 g (with OCXO)

# 7 Installing the syn1588® PCIe NIC Hardware

The following instructions are general installation guidelines. Consult your computer's user manual for specific instructions and warnings for installing new PCI/PCIe components.

**Caution**

The syn1588® PCIe NIC is sensitive to electrostatic discharge that may damage the unit. Please observe ESD protection rules. Do not directly touch the unmounted syn1588® PCIe NIC while not being properly grounded. Use the ESD bags provided by Oregano Systems for shipping and storage.

## 7.1 Installation

- Be sure to have powered–off your PC prior to installing the syn1588® PCIe NIC. Failure to do so could endanger you and may damage the syn1588® PCIe NIC or computer

- Please be sure to thoroughly ground yourself by means of a grounding strap or by touching a grounded object prior to unpacking the syn1588® PCIe NIC card
- Insert the syn1588® PCIe NIC into the empty PCIe slot and verify that the card is properly inserted and fastened by means of levels or screw of the case
- Plug in the power cord of the computer and power the computer on

The syn1588® PCIe NIC card is now installed.

**Caution**

Please note that some BIOS implementations do not allow plugging a 1-lane PCIe card into an 8-lane or 16-lane slot. Please consult your BIOS manual in case of troubles.

# 8 Software

## 8.1 Driver

The syn1588® PCIe NIC requires a driver software for its operation on your host PC. There are drivers available for Linux and Windows for both 32 bit and 64 bit systems. Currently, the following operating systems are officially supported.

| OS |
|---|
| Windows 7/8/10 (x32/x64) [1] |
| Windows 11 (x32/x64) |
| Windows Server 2003/2008/2012 (x32/x64) [1] |
| Windows Server 2016 (x32/x64) |
| Linux kernel version 2.6.32 – 5.15 |

**Table 6 Driver software: supported OS**

Note (1) there is no support for signed drivers for these OS versions. One has to disable secure boot to use the driver on these OS versions. Windows 7 users might need to install KB3033929. Please consult the syn1588® User Guide for further installation instructions.

Please be aware that the current driver versions do not support any power-saving mode like stand-by or hibernation. The syn1588® PCIe NIC needs to be restarted by reloading the driver.

## 8.2 syn1588® PTP Stack

Every syn1588® PCIe NIC comes with a binary run-time license of the syn1588® PTP Stack. The syn1588® PTP Stack is available for both Windows and Linux. The syn1588® PTP Stack supports all operating system versions listed in Table 6 Driver software: supported OS

Please refer to the syn1588® User Guide for more information on using syn1588® software.

# 9 Further Information

You are looking for further information not included in this datasheet? Please contact Oregano Systems support! We will be pleased to provide you all the required information.

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Vienna, October 30th 2022

## Certificate of Conformance

The Oregano Systems Ethernet network interface card with IEEE1588 capabilities "syn1588® PCIe NIC" (board revision 2.3) meets the intent of Electromagnetic Compatibility directive 2014/30/EU, Low Voltage directive 2014/35/EU and safety requirements for electrical equipment for measurement, control and laboratory use.

Compliance was demonstrated to the following specifications:

- EN55032:2015
- EN55035:2017
- FCC Part 15 October 2018 edition
- EN 62368-1:2014 + A11:2017
- IEC 62368-1:2018

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## RoHS Certificate of Conformance

The Oregano Systems' syn1588® products listed below is (are) in compliance with Directive 2011/65/EC and 2015/863/EC on the restriction of the use of certain hazardous substances in electrical and electronic equipment (RoHS and RoHS 3 directives).

- syn1588® Gbit Switch (board revision 1.9)
- syn1588® PCIe NIC Revision 2.1
- syn1588® PCIe NIC Revision 2.3
- syn1588® VIP Evaluation Board Revision 3
- syn1588® Dual NIC Revision 1.0

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## WEEE status of the product

This product is handled as a B2B category product. In order to secure a WEEE compliant waste disposal it has to be returned to the manufacturer. Any transportation expenses for returning this product (at its end of life) have to be incurred by the end user, whereas Oregano Systems will bear the costs for the waste disposal itself.

## RL 94/62/EG status of the packaging material

This packaging material is handled as a B2B category packaging material. In order to secure a RL 94/62/EG compliant waste disposal it has to be returned to the manufacturer. Any transportation expenses for returning this product have to be incurred by the end user, whereas Oregano Systems will bear the costs for the waste disposal itself.

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## Letter of Volatility

The following table shows the non-volatile memories of the syn1588® PCIe NIC – Revision 2.3. Please note that no customer data is stored in these non-volatile memories.

| memory | function | size | writeable | user R/W | access restriction |
|---|---|---|---|---|---|
| SPI Flash<br>U17<br>Micron<br>MT25QL128ABA8E12 | FPGA configuration storage | 128Mbit | yes | no | dedicated firmware update software required, only user configuration may be written, factory default configuration is write protected in hardware |
| I2C EEPROM<br>U1<br>ON Semiconductor<br>CAT24AA01TD[1] | MAC address | 1kbit | no | no | no write access implemented in hardware |

Note (1): the functional compatible device CAT24AA16TD (16 kbit) might optionally be populated instead.

Gerhard R. Cadek
(CEO)

| IEC IECEE CB SCHEME | Ref. Certif. No. |
|---|---|
| | **AT 4251** |

IEC SYSTEM FOR MUTUAL RECOGNITION OF TEST CERTIFICATES FOR ELECTRICAL EQUIPMENT (IECEE) CB SCHEME

## CB TEST CERTIFICATE

| | |
|---|---|
| Product | **PCI Express Ethernet network interface card** |
| Name and address of the applicant | **Oregano Systems - Design & Consulting GesmbH**<br>**Franzosengraben 8,**<br>**1030 Wien, Austria** |
| Name and address of the manufacturer | **Oregano Systems - Design & Consulting GesmbH**<br>**Franzosengraben 8,**<br>**1030 Wien, Austria** |
| Name and address of the factory<br>*Note: When more than one factory, please report on page 2* | **technosert electronic GmbH**<br>**Angererweg 7,**<br>**4224 Wartberg ob der Aist, Austria**<br>☐ Additional Information on page 2 |
| Ratings and principal characteristics | **3,3Vdc / 1A; 12Vdc / 0,2 A** |
| Trademark (if any) | **Oregano Systems** |
| Customer's Testing Facility (CTF) Stage used | -- |
| Model / Type Ref. | **syn1588 -PCIe NIC** |
| Additional Information (if necessary may also be reported on page 2) | --<br>☐ Additional Information on page 2 |
| A sample of the product was tested and found to be in conformity with | **IEC 62368-1:2018** |
| As shown in the Test Report Ref. No. which forms part of this Certificate | **INE-AT/IT-19/134** |

This CB Test Certificate is issued by the National Certification Body

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Testing and Certification
Kahlenberger Str. 2A, 1190 Wien, Austria

Digitally signed by W. Martin
Email=w.martin@ove.at

Date: 2019-10-22

Signature: Dipl.-Ing. W. Martin

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