

syn1588<sup>®</sup>

PCI Express Ethernet Network Interface Card

# syn1588<sup>®</sup> 10G NIC

Data Sheet – Advance Information

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**Oregano Systems – Design & Consulting GesmbH**  
A Meinberg Company

Franzosengraben 8, A-1030 Vienna

P: +43 (676) 84 31 04-360

@: [contact@oregano.at](mailto:contact@oregano.at)

W: <http://oregano.at>

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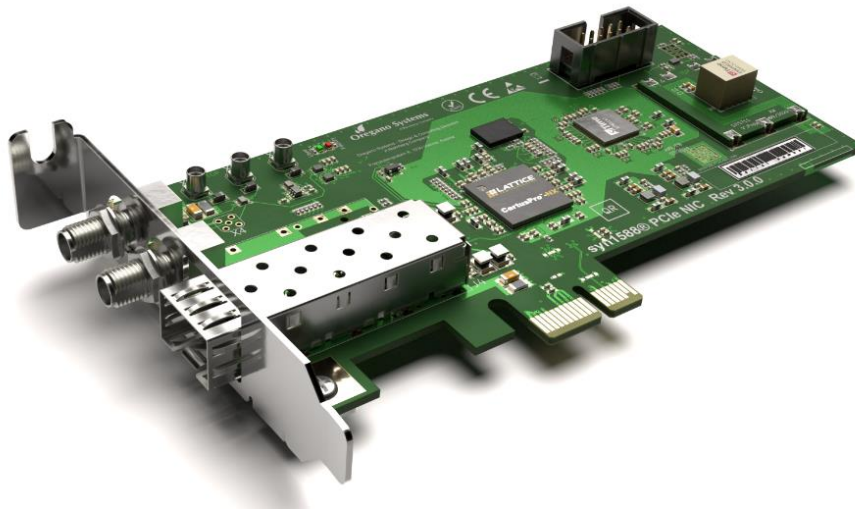
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# 1 Overview

## 1.1 Functional description

The syn1588® 10G NIC is a 10 Gbit Ethernet network interface card (1-lane PCI Express low-profile card) with enhancements to provide the network node with accurate clock synchronization via Ethernet following the IEEE1588 standard.



**Figure 1: syn1588® 10G NIC**

The syn1588® 10G NIC is using the Oregano Systems syn1588® technology for time stamping of arbitrary network packets. The timestamping unit is fully user configurable enabling any type of packet timing application. The syn1588® 10G NIC provides full support for IEEE1588-2002 as well as IEEE1588-2008 specific features like the patented on-the-fly timestamping mechanism (one-step mode). The syn1588® 10G NIC is based on the Revision 3 of the syn1588® PCIe NIC. It offers on a 10 Gbit network the same accurate and comfortable clock synchronization functions our customers are used from our existing syn1588® NICs.

The syn1588® 10G NIC is designed for 10 Gbit network connectivity but not offering full 10 Gbit bandwidth. In many user scenarios there are no more 1000 Mbit network ports available to attach a PTP timing card. That's where this card provides a solution. Note, although the card provides 10 Gbit line speed its power consumption is very low. Thus, no special cooling is required.

## 2 Features

The following features are based on the hardware build ID 525 of the syn1588® 10G NIC. Other build versions of the syn1588® 10G NIC will offer somewhat different capabilities. Please contact Oregano Systems support for details.

### 2.1 NIC Features

- Standard 10 Gbps Ethernet network card following IEEE802.3-2015
- 1-lane PCI Express (PCIe) low-profile card
- Compliant to PCI Express version 3.0 (8 Gbit/s)
  - Compatible with PCI Express version 2 (5 Gbit/s)
  - Compatible with PCI Express version 1.1 (2.5 Gbit/s)
- SFP+ type network interface
  - Supporting 10GBASE-SR (fiber SFP+ transceiver modules)
- 16 kbyte Ethernet transmit FIFO buffer, 64 kbyte Ethernet receive FIFO buffer
- VLAN and IPv6 support
- Promiscuous mode supported
- Driver software available for Linux and Windows. Both 32 bit and 64 bit systems are supported.

## 2.2 IEEE1588 Features<sup>1</sup>

- Fully IEEE1588-2002, IEEE1588-2008 and IEEE1588-2019 compliant
- Support for Oregano Systems' patented syn1588® technology:
- On-the-fly timestamping while sending or receiving time sync packets (1-step mode)
- IEEE1588 hardware clock
  - utilizes IEEE1588 time format
  - fully maintained in hardware
- Clock servo operation is controlled by the software without real-time requirements
- Software does not need to execute time format conversion
- syn1588® clock frequency is 125 MHz
- All real-time functions for IEEE1588 are implemented in hardware eliminating real-time constraints for the syn1588® PTP Stack
- IEEE1588 master and slave operation supported<sup>2</sup>
- High quality TCXO oscillator
  - Initial tolerance: 1ppm or better
  - Holdover performance: 0.28 ppm for 24h
- Optional high-stability OCXO oscillator
  - Initial tolerance: 0.5ppm
  - Holdover performance: Stratum 3E compliant
- Up to four programmable input/output signals available on SMA connectors
  - 50  $\Omega$ , 3V3 LVCMOS signalling
- 1PPS input and/or output<sup>3</sup>
- Up to two EVENT inputs
- Up to two TRIGGER outputs
- Up to two+two<sup>4</sup> PERIOD outputs
- Optional clock input to drive the syn1588® clock for selected clock frequencies
- Programmable interrupt conditions
- IRIG-B007 output data stream generation (DCLS signal, no carrier, BCD + BCD\_Year + SBS)
- Optional IRIG-B007 input decoding (DCLS signal, no carrier, BCD + BCD\_Year)
- On-board jitter cleaner PLL for generating accurate, synchronized single-ended frequencies up to 156.25 MHz

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<sup>1</sup> Requires the Oregano Systems syn1588® PTP Stack to run the protocol engine.

<sup>2</sup> Oregano Systems generally recommends using the high-stability OCXO option for all master applications.

<sup>3</sup> Constant delay of three clock periods to the external output signal. Minimum pulse width is 100  $\mu$ s.

<sup>4</sup> Beside the two standard PERIOD functions there are two PERIOD light functions available

- Connectivity to an external GPS receiver via the 1 PPS input as well as a serial port of the host PC for external synchronization
  - Serial port not included in the syn1588® 10G NIC
  - NMEA-0183 RMC messages required
- Binary run-time license for syn1588® PTP Stack included
- Several utilities are available for accessing registers, synchronizing the node's system clock, or synchronizing to an external GPS receiver.
- Software APIs are available allowing the user to write custom software including interrupt service routines accessing the syn1588® functions, accessing all hardware clock related functions and controlling/observing the syn1588® PTP Stack
- syn1588® Linux Live System for fast testing of the syn1588® 10G NIC without the need of software installation. Just install the syn1588® 10G NIC in your node and boot the PC using the syn1588® Linux Live System

### 2.2.1 Timestamping

- Programmable timestamping unit on Ethernet receive and transmit path for time stamping IEEE1588 packets
- Independent timestamp FIFOs for Ethernet receive path and transmit path (256 words each) allows timestamping of multiple dense packets without losing data thus removing the software real-time requirements
- Patented on-the-fly timestamping for 1-step operation on Ethernet transmit path
- Timestamping supported for VLAN as well as IPv6 operation
- Timestamping of two external input signals – EVENT: On the rising edge of these external signals a timestamp will be drawn
- For EVENT0 input a 16-entry timestamp FIFO is implemented allowing timestamping of dense events with a distance of just 100 ns
- Extremely high timestamp resolution of 4 ns



## 2.2.2 User Programmable Events

- TRIGGER: Two user programmable single event output signals may be generated
- These TRIGGER signals change their respective state at a programmable time that is derived from the highly accuracy IEEE1588 hardware clock
- TRIGGER0 output is controlled by a 16-entry FIFO providing support for dense event sequences without imposing real-time requirements on the software
- Resolution of all TRIGGER events is +/-4 ns
- Maximum TRIGGER event duration is 32 bit seconds
- PERIOD: Two user programmable periodical output signals may be generated that are derived from the highly accuracy IEEE1588 hardware clock
- The frequency may be selected in the range of mHz to 156.25 MHz
- The resolution of all PERIOD events is  $2^{-16}$  ns, i.e. 0,0153 ps
- The maximum PERIOD duration is 65535 seconds (16 bit)

## 2.3 Hardware Options

- High-stability OCXO for master operations or high accuracy applications.
- External clock input for the PTP hardware clock

### 3 Block Diagram

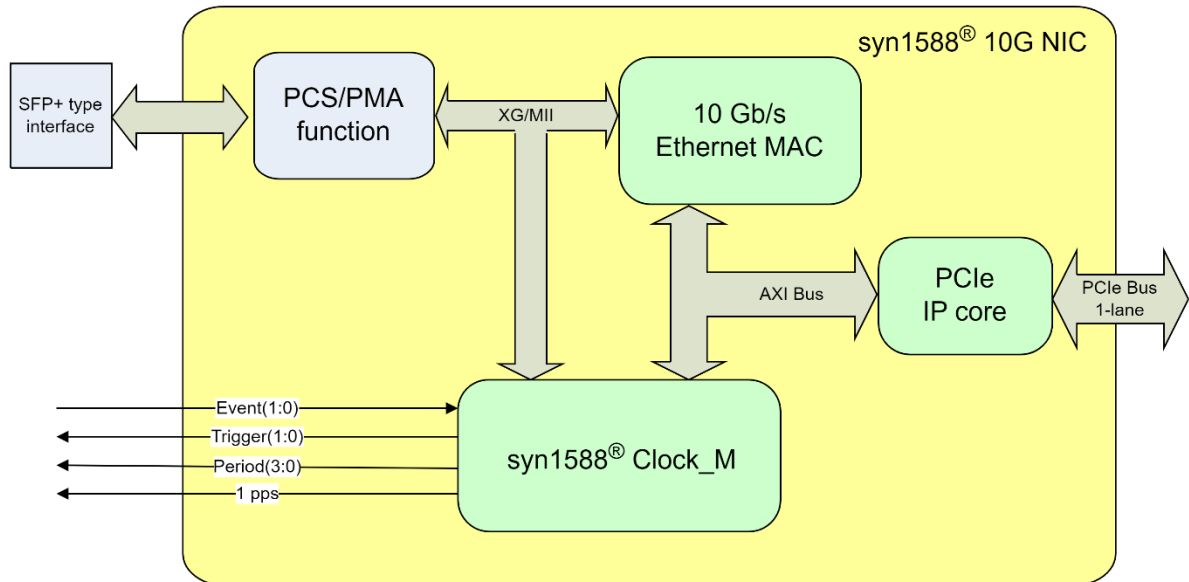


Figure 2: syn1588® 10G NIC: block diagram

The syn1588® 10G NIC basically consists of a single FPGA containing the following IP cores:

- 10 Gbps Ethernet Media Access Controller (MAC)
- syn1588® Clock\_M IP Core
- PCIe interface
- PCS/PMA function

## 4 Mechanics

The following figure shows the dimensions of the syn1588® 10G NIC.

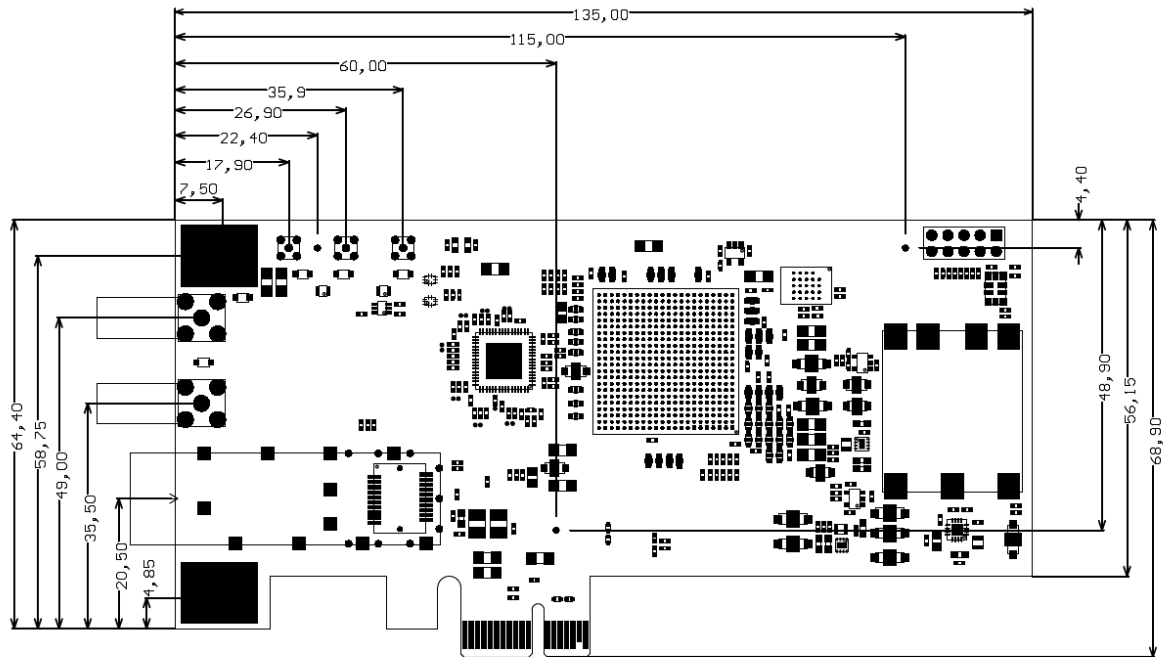
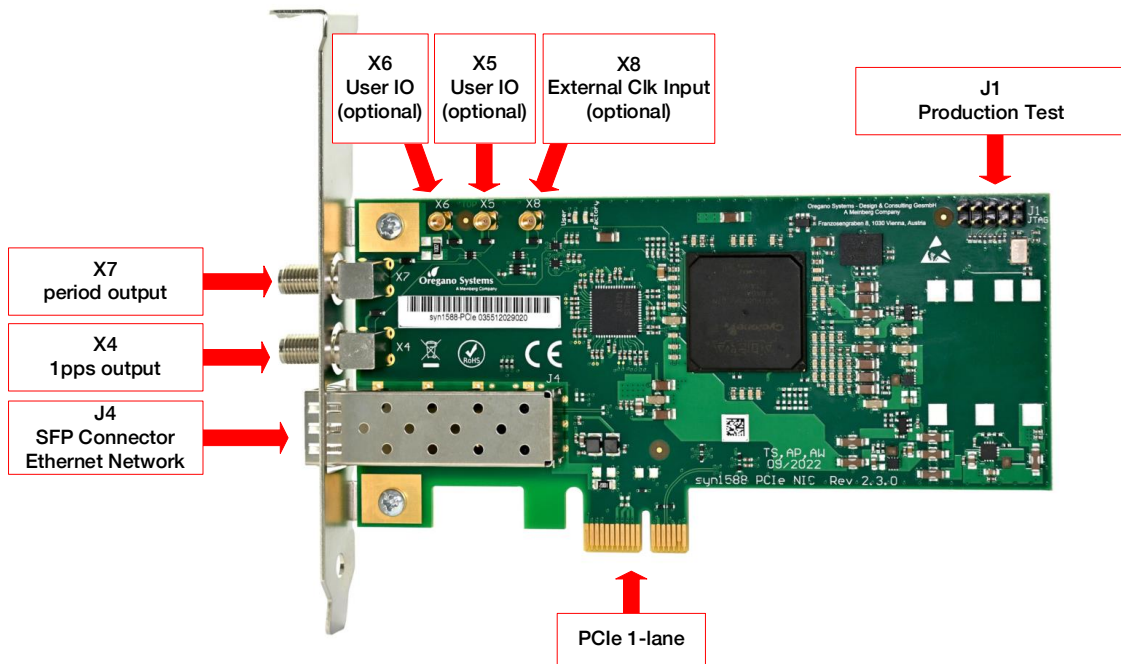


Figure 3: syn1588® 10G NIC: dimensions & placement of connectors (all dimensions are in mm)



**Figure 4: syn1588® 10G NIC: connectors**

Oregano Systems offers two different types of brackets for the syn1588® 10G NIC to facilitate any type of mounting situation; the card comes with both brackets.

- Low-profile bracket with 2 SMA connectors (default option, mounted)
- Standard bracket with 2 SMA connectors

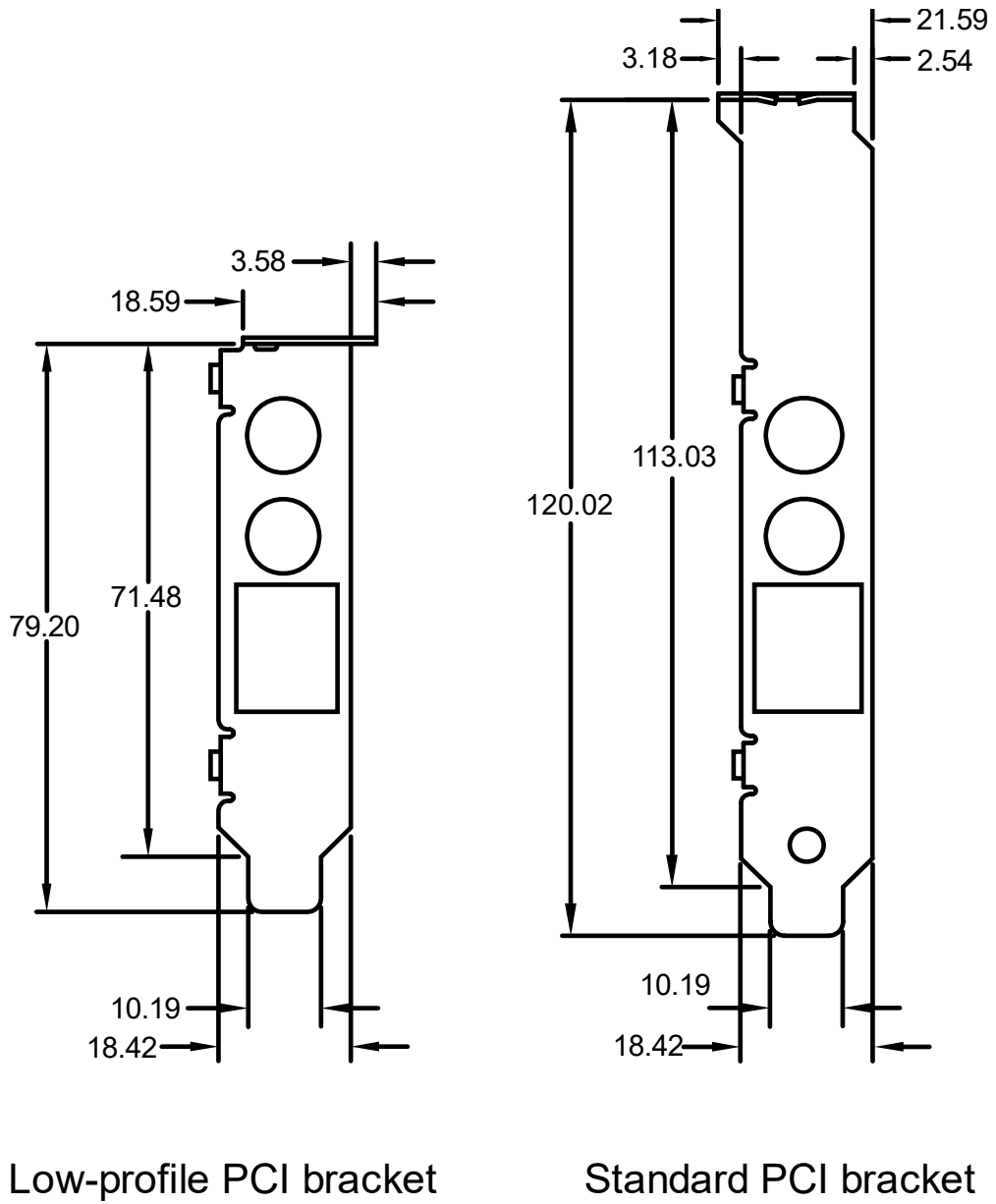


Figure 5: PCI bracket options

## 5 Electrical Interface Specification

### 5.1 ESD

All user accessible connectors of the syn1588® 10G NIC are protected against ESD damage following IEC61000-4-2 15 kV air 8 kV contact.

### 5.2 Power Supply

The syn1588® 10G NIC board is operated using the 3V3 power supplied by the PCI Express edge connector. The oscillators – the TCXO as well as the optional OCXO - are powered by highly stable on-board supply which uses the 12V supplied by the PCI Express edge connector.

DC Characteristics	
Minimum DC 3V3 input voltage	3.0 V
Maximum DC 3V3 input voltage	3.6 V
Maximum DC supply current @ 3,3 V	1.0 A
Minimum DC 12V input voltage	11.5 V
Maximum DC 12V input voltage	12.5 V
Maximum DC supply current @ 12V	0.2 A

**Table 1 Power supply DC characteristics**

### 5.3 SFP+ Ethernet Interface (J4)

The SFP+ interface supports 10GBASE-SR mode using the following SFP+ transceiver modules.

Vendor	Type	Mode	Range	Connector	Order Number
Fiberstore	fiber	multi	SR	LC	SFP-10GSR-85
10Gtek	fiber	multi	SR	LC	AXS85-192-M3

**Table 2 Supported SFP transceiver modules**

All fiber SFP+ transceiver modules use the LC connector. Using other compatible SFP+ transceiver modules (including LR modules) might work as well but will neither be officially supported nor tested.

## 5.4 User Interface (X4, X5, X6, X7)

There are four connectors available for the user: two SMA at the PCI bracket and two MMCX connectors on board. The function and direction for every of the four connectors is configurable by the user during run-time using the syn1588® Software Suite.

The default configuration of these user IOs is as follows:

- X4: 1 PPS
- X7: period\_0 output signal
- X6: event\_0 input signal
- X5: disabled

The output signals deliver a standard 3V3 level 50  $\Omega$  output signal driving a maximum of 20 mA. The input signals expect a standard 3V3 level signal. The output signals may drive two or three standard loads when using correct 50  $\Omega$  cabling.

Two SMA connectors (X4 and X7) are directly available at the PCI bracket while two more connectors (X5 and X6) are available internally. Upon request (via the appropriate ordering code) Oregano Systems supplies the cable to directly connect to a SMA port.

### 5.4.1 SMA Output Characteristics

<b>Output coupling</b>	DC
<b>Output threshold high</b>	2.8 V min
<b>Output threshold low</b>	0.4 V max
<b>Absolute maximum applied voltage</b>	-0 V to 3.465 V
<b>Output to output skew, synchronous</b>	< 1 ns typical
<b>Output current</b>	±20 mA max

Table 3 SMA Output Characteristics

### 5.4.2 SMA Input Characteristics

<b>Input impedance</b>	50 $\Omega$ nominal
<b>Input coupling</b>	DC
<b>Voltage level</b>	0 to 3.3 V
<b>Absolute maximum input voltage</b>	-0.5 V to 4.25 V
<b>Minimum pulse width</b>	500 ns
<b>Input threshold high</b>	2.0 V
<b>Input threshold low</b>	0.8 V

Table 4 SMA Input Characteristics

## 5.5 External clock Input Interface (X8)

Optionally there is an external clock input available to allow direct driving the syn1588® hardware clock from this external signal.

<b>Input impedance</b>	50 $\Omega$ nominal
<b>Input coupling</b>	DC
<b>Voltage level</b>	0 to 3.3 V
<b>Absolute maximum input voltage</b>	-0.5 V to 4.25 V
<b>Input threshold high</b>	2.0 V
<b>Input threshold low</b>	0.8 V

Table 5 External Clock Input Characteristics

The ExtClk input is a digital input and thus cannot accept sinewave signals etc. A duty cycle of 30-70 % is required.

## 5.6 Production Test (J1)

The production test connector must be left unconnected while the syn1588® 10G NIC is operated. Note that there is no special ESD protection for this interface.



## **6 Environmental**

### **6.1 Temperature**

Operating temperature range 0° C ... +50° C

Storage temperature range -40° C ... +85° C

### **6.2 Humidity**

Operating humidity 5% to 80% RH, non-condensing

### **6.3 Weight**

Total weight approx. 70 g (without OCXO)

Total weight approx. 75 g (with OCXO)

## 7 Installing the syn1588® 10G NIC Hardware

The following instructions are general installation guidelines. Consult your computer's user manual for specific instructions and warnings for installing new PCI/PCIe components.

### Caution

The syn1588® 10G NIC is sensitive to electrostatic discharge that may damage the unit. Please observe ESD protection rules. Do not directly touch the unmounted syn1588® 10G NIC while not being properly grounded. Use the ESD bags provided by Oregano Systems for shipping and storage.

### 7.1 Installation



- Be sure to have powered-off your PC prior to installing the syn1588® 10G NIC. Failure to do so could endanger you and may damage the syn1588® 10G NIC or computer



- Please be sure to thoroughly ground yourself by means of a grounding strap or by touching a grounded object prior to unpacking the syn1588® 10G NIC card
- Insert the syn1588® 10G NIC into the empty PCIe slot and verify that the card is properly inserted and fastened by means of levels or screw of the case
- Plug in the power cord of the computer and power the computer on

The syn1588® 10G NIC card is now installed.

### Caution

Please note that some BIOS implementations do not allow plugging a 1-lane PCIe card into an 8-lane or 16-lane slot. Please consult your BIOS manual in case of troubles.

## 8 Software

### 8.1 Driver

The syn1588® 10G NIC requires a driver software for its operation on your host PC. There are drivers available for Linux and Windows for both 32 bit and 64 bit systems. Currently, the following operating systems are officially supported.

OS
Windows 10 (x32/x64) <sup>1</sup>
Windows 11 (x32/x64)
Windows Server 2008/2012 (x32/x64) <sup>1</sup>
Windows Server 2016 (x32/x64)
Linux kernel version 3.x – 5.15

**Table 6 Driver software: supported OS**

Note (1) there is no support for signed drivers for these OS versions. One has to disable secure boot to use the driver on these OS versions. Windows 7 users might need to install KB3033929. Please consult the syn1588® User Guide for further installation instructions.

Please be aware that the current driver versions do not support any power-saving mode like stand-by or hibernation. The syn1588® 10G NIC needs to be restarted by reloading the driver.

### 8.2 syn1588® PTP Stack

Every syn1588® 10G NIC comes with a binary run-time license of the syn1588® PTP Stack. The syn1588® PTP Stack is available for both Windows and Linux. The syn1588® PTP Stack supports all operating system versions listed in Table 6 Driver software: supported OS

Please refer to the syn1588® User Guide for more information on using syn1588® software.

## 9 Further Information

You are looking for further information not included in this datasheet? Please contact Oregano Systems support! We will be pleased to provide you all the required information.



Franzosengraben 8

A-1030 Vienna

AUSTRIA

<https://oregano.at>

[contact@oregano.at](mailto:contact@oregano.at)

**Oregano Systems - Design & Consulting GesmbH**  
Franzosengraben 8, 1030 Vienna, Austria

Phone: +43 (676) 843104 200  
Mail: [contact@oregano.at](mailto:contact@oregano.at)  
Web: [www.oregano.at](http://www.oregano.at)

AW | @ wingelhofer@oregano.at | +43 676 84 31 04-550

Vienna, June 30<sup>th</sup> 2024

## Certificate of Conformance

The Oregano Systems Ethernet network interface card with IEEE1588 capabilities “syn1588® 10G NIC” meets the intent of Electromagnetic Compatibility directive 2014/30/EU, Low Voltage directive 2014/35/EU and safety requirements for electrical equipment for measurement, control and laboratory use.

Compliance was demonstrated to the following specifications:

- EN55032:2015
- EN55035:2017
- FCC Part 15 October 2018 edition
- EN 62368-1:2014 + A11:2017
- IEC 62368-1:2018

Alexander Wingelhofer  
(CEO)

**Oregano Systems - Design & Consulting GesmbH**  
Franzosengraben 8, 1030 Vienna, Austria

Phone: +43 (676) 843104 200  
Mail: [contact@oregano.at](mailto:contact@oregano.at)  
Web: [www.oregano.at](http://www.oregano.at)

AW | @ wingelhofer@oregano.at | +43 676 84 31 04-550

Vienna, June 30<sup>th</sup> 2024

## RoHS Certificate of Conformance

The Oregano Systems' syn1588<sup>®</sup> products listed below is (are) in compliance with Directive 2011/65/EC and 2015/863/EC on the restriction of the use of certain hazardous substances in electrical and electronic equipment (RoHS and RoHS 3 directives).

- syn1588<sup>®</sup> Gbit Switch (board revision 1.9)
- syn1588<sup>®</sup> PCIe NIC Revision 2.1
- syn1588<sup>®</sup> PCIe NIC Revision 2.3
- syn1588<sup>®</sup> 10G NIC
- syn1588<sup>®</sup> VIP Evaluation Board Revision 3
- syn1588<sup>®</sup> Dual NIC Revision 1.0

Alexander Wingelhofer  
(CEO)

**Oregano Systems - Design & Consulting GesmbH**  
Franzosengraben 8, 1030 Vienna, Austria

Phone: +43 (676) 843104 200  
Mail: [contact@oregano.at](mailto:contact@oregano.at)  
Web: [www.oregano.at](http://www.oregano.at)

AW | @ wingelhofer@oregano.at | +43 676 84 31 04-550

Vienna, June 30<sup>th</sup> 2024

### **WEEE status of the product**

This product is handled as a B2B category product. In order to secure a WEEE compliant waste disposal it has to be returned to the manufacturer. Any transportation expenses for returning this product (at its end of life) have to be incurred by the end user, whereas Oregano Systems will bear the costs for the waste disposal itself.

### **RL 94/62/EG status of the packaging material**

This packaging material is handled as a B2B category packaging material. In order to secure a RL 94/62/EG compliant waste disposal it has to be returned to the manufacturer. Any transportation expenses for returning this product have to be incurred by the end user, whereas Oregano Systems will bear the costs for the waste disposal itself.

Alexander Wingelhofer  
(CEO)

**Oregano Systems - Design & Consulting GesmbH**  
Franzosengraben 8, 1030 Vienna, Austria

Phone: +43 (676) 843104 200  
Mail: [contact@oregano.at](mailto:contact@oregano.at)  
Web: [www.oregano.at](http://www.oregano.at)

AW | @ wingelhofer@oregano.at | +43 676 84 31 04-550

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## Letter of Volatility

The following table shows the non-volatile memories of the syn1588<sup>®</sup> 10G NIC. Please note that no customer data is stored in these non-volatile memories.

memory	function	size	writeable	user R/W	access restriction
SPI Flash U17 Micron MT25QL128ABA8E12	FPGA configuration storage	128Mbit	yes	no	dedicated firmware update software required, only user configuration may be written, factory default configuration is write protected in hardware
I2C EEPROM U1 ON Semiconductor CAT24AA01TD <sup>1</sup>	MAC address	1kbit	no	no	no write access implemented in hardware

Note (1): the functional compatible device CAT24AA16TD (16 kbit) might optionally be populated instead.

Alexander Wingelhofer  
(CEO)





Ref. Certif. No.

**AT 4251**

IEC SYSTEM FOR MUTUAL RECOGNITION OF TEST CERTIFICATES FOR ELECTRICAL EQUIPMENT (IECEE) CB SCHEME

**CB TEST CERTIFICATE**

Product	PCI Express Ethernet network interface card
Name and address of the applicant	Oregano Systems - Design & Consulting GesmbH Franzosengraben 8, 1030 Wien, Austria
Name and address of the manufacturer	Oregano Systems - Design & Consulting GesmbH Franzosengraben 8, 1030 Wien, Austria
Name and address of the factory	technosert electronic GmbH Angererweg 7, 4224 Wartberg ob der Aist, Austria
Note: When more than one factory, please report on page 2	<input type="checkbox"/> Additional Information on page 2
Ratings and principal characteristics	3,3Vdc / 1A; 12Vdc / 0,2 A
Trademark (if any)	Oregano Systems
Customer's Testing Facility (CTF) Stage used	-
Model / Type Ref.	syn1588 -PCIe NIC
Additional Information (if necessary may also be reported on page 2)	-
	<input type="checkbox"/> Additional Information on page 2
A sample of the product was tested and found to be in conformity with	IEC 62368-1:2018
As shown in the Test Report Ref. No. which forms part of this Certificate	INE-AT/IT-19/134

This CB Test Certificate is issued by the National Certification Body



**Österreichischer Verband für Elektrotechnik**  
Testing and Certification  
Kahlenberger Str. 2A, 1190 Wien, Austria



Date: 2019-10-22

*W. Martin*

Digitally signed by W. Martin  
Email=w.martin@ove.at

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