Version 1.3

MC8051 IP Core

Oregano Systems 8-bit Microcontroller IP-Core

Key Features

- Fully synchronous design
- Technology independent, clear structured, well commented VHDL source code
- Easily expandable by adapting/changing VHDL source code
- Parametrizeable design by simply changing VHDL constants
- User selectable number (N) of timers/counters and serial interface units
- Active timer/counter and serial interface units selected by additional special function register
- Instruction set compatible to the industry standard 8051 microcontroller
- Up to 10 times faster due to completely new architecture
- Optional implementation of the multiply command (MUL) using a parallel multiplier
- Optional implementation of the divide command (DIV) using a parallel divider
- Optional implementation of the decimal adjustment command (DA)
- No multiplexed I/O ports
- 256 bytes internal RAM
- Up to 64 kbyte ROM, up to 64 kbyte RAM
- Source code available free of charge under the GNU LGPL license

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Block Diagram

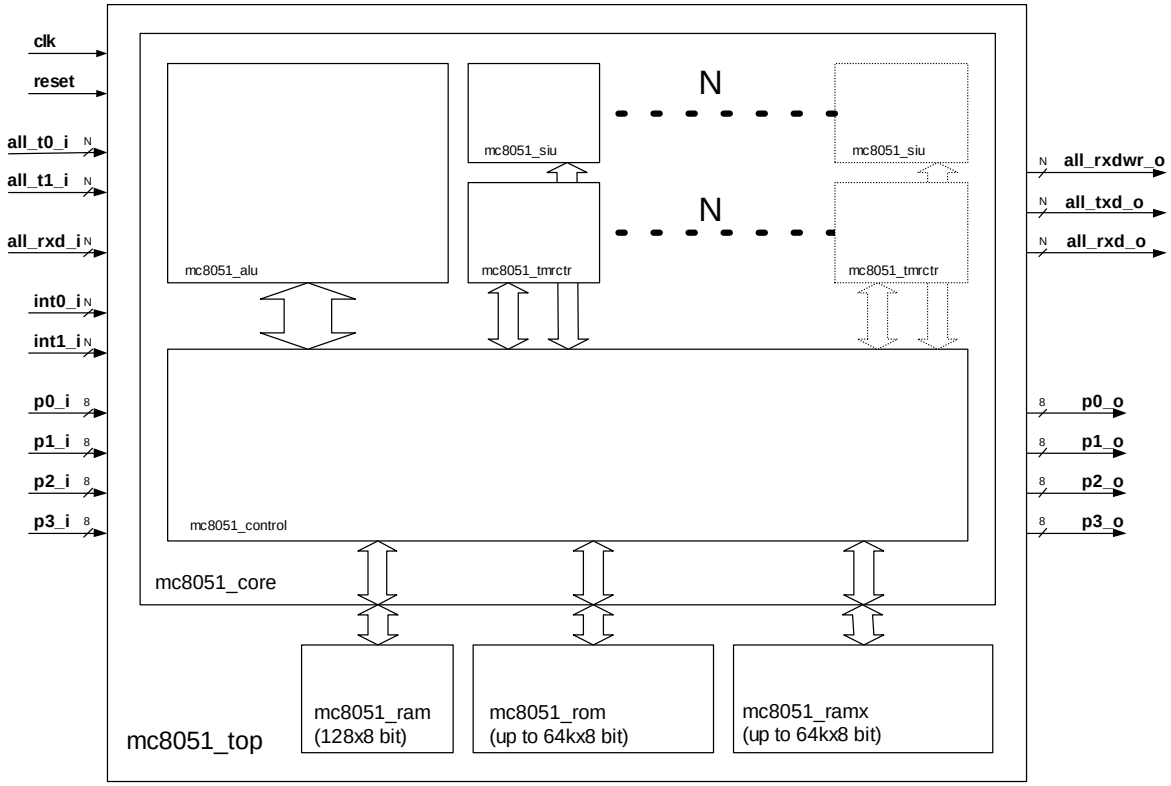

Fig 1. Block diagram: 8051 microcontroller IP core

Beside the 8051 IP core that is available free of charge Oregano Systems' also offers an industrial license of this 8051 IP core.

The industrial license of the well-known 8051 IP core includes the following additional features.

- 1-step pipelining for reading the ROM
- standard ROM banking via SFR register (0xB1) allows ROM sizes greater than 64 kbytes, banking automatically supported e.g. by IAR compiler
- 64 bit ALU supporting the operations add, subtract, multiply, shift left/right, 64 bit ALU enabled via constants in the 8051 package
- double precision floating point ALU (IEEE 754 compliant) supporting the operations add, subtract, multiply, divide,
  ALU based on the OpenCores FPU by David Lundgren,
  FPU ALU enabled via constants in the 8051 package
- RAMX DMA unit

Document Revisions

- Version 1.0, December 2001: Initial document describing the main properties of the mc8051 core.
- Version 1.1, January 2002: Added the block diagram.
- Version 1.2, June 2002: Corrected names of ports in the block diagram to correspond to the VHDL source code.
- Version 1.3, June 2013: Changed mail address and internet link, added description of industrial 8051 IP core