Version 1.9 – March 2019

Abstract

This application note presents an overview on the basic features of Oregano Systems' syn1588® IP Cores.

syn1588® IP Cores

The following tables compares the basic features of the syn1588® IP cores offered by Oregano Systems.

Parameter	syn1588® Clock_M	syn1588® VIP
Basic Features		
requires external software/processor (syn1588® PTP Stack)	yes	no
requires real-time capable software	no	no
full access to all time registers	yes	no
suited for high event rate	yes	yes
single chip solution	no	yes
suited for SoC designs	yes	yes
FPGA net list license	yes	yes
VHDL source code license	yes	yes
evaluation board available	yes[1]	yes[2]
remote configuration/access	yes[3]	yes

Table 1 syn1588® IP core – Basic features

Notes:

(1) syn1588® PCIe NIC

(2) syn1588® VIP Eval Board

(3) when running Oregano Systems' syn1588® PTP Stack

	syn1588®Clock_M	syn1588® VIP
Basic Parameters		
external interface	AXI, GMII, XGMII, 25GMII	MII/GMII, RS232
external/internal interrupts	1/15	-/15
trigger outputs	1/2	-/1
trigger outputs with FIFO to avoid dead time	1	-/1
period timer outputs	2	1
event inputs	2	1
event inputs with FIFO for high frequency events	1	1
separate 1 PPS output	1	1
IRIG-B output	X	X
IPv6 capable	X	-
IPv6 support for 1-step mode	X	-
IEEE1588 TIME register sets	1/2	1
IEEE1588 clock core width [bit]	96	96
IEEE1588 clock resolution [ns]	2^{-32}	2^{-32}
timer / event precision [bit]	64/64	64/64
timestamping units	1/2	1/2
on-the-fly timestamping support	-/1[1]	-/1[1]
separate RX & TX timestamp FIFOs	X	X
timestamp FIFO TX depth [Entries]	16	16
timestamp FIFO RX depth [Entries]	256	256
timestamp FIFO stores packet ID	X	X
timestamp FIFO full/empty flag	X/X	X/X

Table 2 syn1588® IP cores: Features at a glance

Legend:

X … supported

+ … partly supported

- … not supported

(1) supported by selectable design options

Typical Applications

This section describes typical application scenarios for each of the IP cores.

syn1588® Clock_M

The syn1588® Clock_M IP Core may be implemented in a FPGA or ASIC to enhance an internal or external microprocessor or microcontroller with IEEE1588 clock synchronization. The parallel AXI interface allows fast data transfer between the processor and the syn1588® Clock_M and thus is suited for high event rates. Beside the AXI interface for controlling the syn1588® Clock_M the GMII/XGMII/25GMII bus has to be connected to the syn1588® Clock_M. The syn1588® Clock_M may act just as an observer on these lines (two-step mode) or may insert timestamps on-the-fly into IEEE1588 packets in transmit direction.

Since the syn1588® Clock_M IP Core is connected via a parallel bus to the processor the processor may access any syn1588® Clock_M IP Core register.

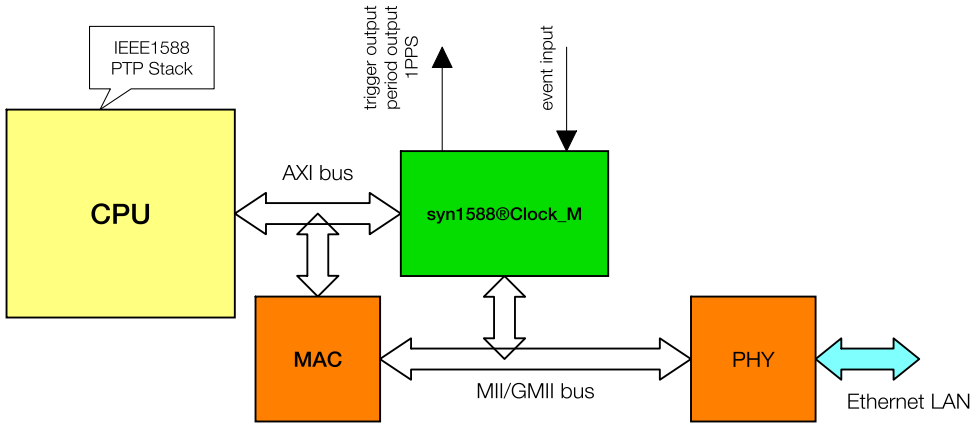

Figure 1 Typical usage of syn1588® Clock_M

The microprocessor has to execute the IEEE1588 PTP Stack software (e.g. Oregano Systems' syn1588® PTP Stack). Running this software service causes just a small load even for a simple microcontroller. The software service does not require a full operating system; a simple IP stack is sufficient.

The syn1588® Clock_M IP core is available in different flavors.

- There is the basic version with a single 100/1000 Mbit network interface syn1588® Clock_M.
- There is a version with up to 5 independent network interfaces (100/1000 Mbit line speed each) sharing the same hardware clock engine named syn1588® Clock_MX.
- Both versions are available with 10 Gbit network interface(s) named syn1588® Clock_M_10G and syn1588® Clock_MX_10G respectively.
- Both versions are available with 25 Gbit network interface(s) named syn1588® Clock_M_25G and syn1588® Clock_MX_25G respectively.

syn1588® VIP

The syn1588® VIP IP core may be implemented in an FPGA or ASIC. The syn1588® VIP acts as a single-chip IEEE1588 node. Just an external Ethernet PHY is required; there is no external CPU or memory required. The syn1588® PTP Stack as well as an simple IP stack is executed onto a 8 bit microcontroller embedded in the syn1588® VIP IP Core.

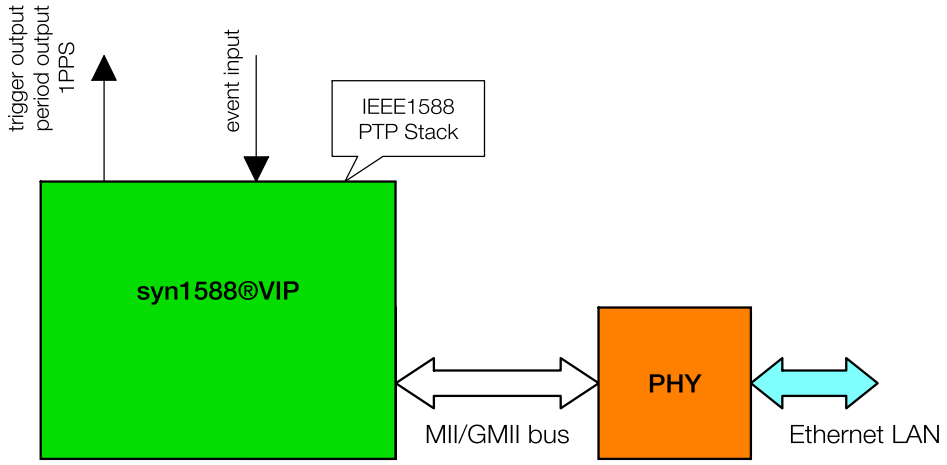

Figure 2 Typical usage of syn1588® VIP

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