FPGA Design Using VHDL

Advanced Methodologies

Your Trainer

Oregano Systems

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Motivation

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- Improve your existing VHDL knowledge
  - Advanced VHDL syntax
    - Design re-usage & team design
    - Efficient verification
- Complex Synthesis Design Flow
- Simulation – The Key for Success

The Course

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- The following time table gives an outline of the course
  - This is just a guideline
- We will focus on the areas of YOUR interest
- Discussions are very important – please ask !
- There is enough time for coffee breaks to relax
  - We may insert a break whenever YOU need one.

Have fun !

Schedule – Day 1

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08:30-10:00 More VHDL Syntax

10:30-12:00 LAB: State Machine Design

13:00-14:30 Dedicated Synthesis Tools
LAB: Combinatorial Divider Unit

15:00-17:30 LAB: Combinatorial Divider Unit – Part II
IP Core Design Flow - LAB: FIR Unit

Schedule – Day 2

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08:30-10:00 Design Constraints

10:30-12:00 Coding Style Guide

Efficient Testbenches using VHDL File IO

13:00-14:30 LAB: File IO

15:00-17:30 LAB: Modeling Memories