Oregano Systems
A Meinberg Company

Parametrizeable ADPCM IP Core

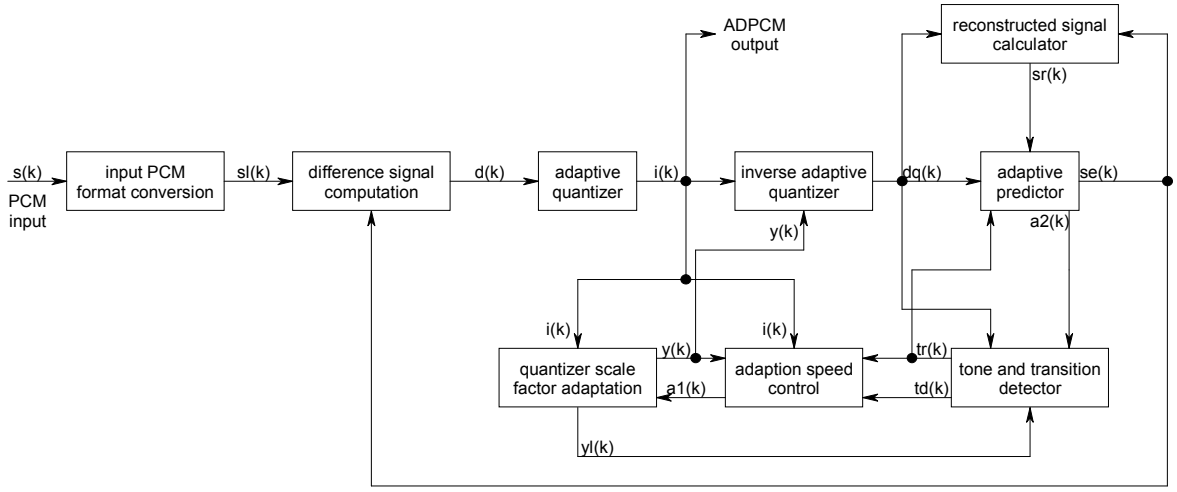
This document describes the features of the parametrizeable ADPCM IP core developed by Oregano Systems.

Features

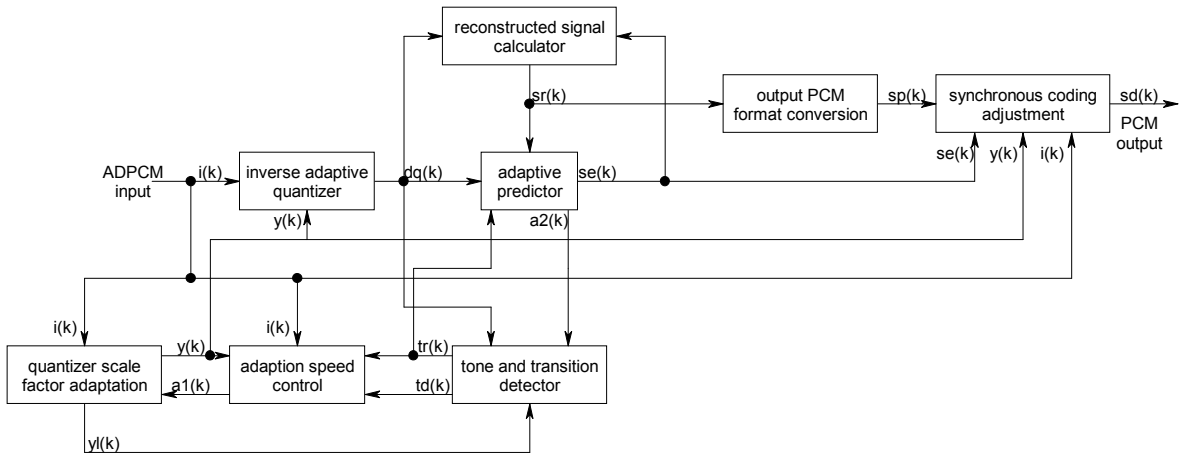
- ADPCM encoder/decoder following ITU G.726
- support of 16/24/32/40 kbit/s operation selectable on a per-channel basis
- support of linear PCM as well as A-law or µ-law coded PCM selectable on a per-channel basis
- configurable number of channels
- channel number just limited by the achieveable speed in the selected target technology
- each channel may be operated either as ADPCM encoder or decoder
- synchronous serial or parallel interface
- any custom interface may be added upon request
- fully synchronous single clock circuit design
- technology independent solution suited for both FPGAs and ASIC technology
- optimized circuit architecture for low clock frequencies and for low memory/logic resource requirements
- support for ITU G.727 available on request

Description

The following figures shows the ADPCM encoder and decoder block diagram as specified in the ITU standard G.726.



ADPCM encoder – block diagram

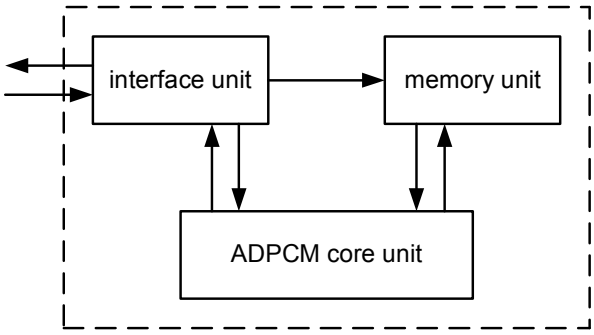


ADPCM encoder – block diagram

The parametrizeable ADPCM IP core is made up of three major design units:

- interface unit
- memory unit
- ADPCM core unit

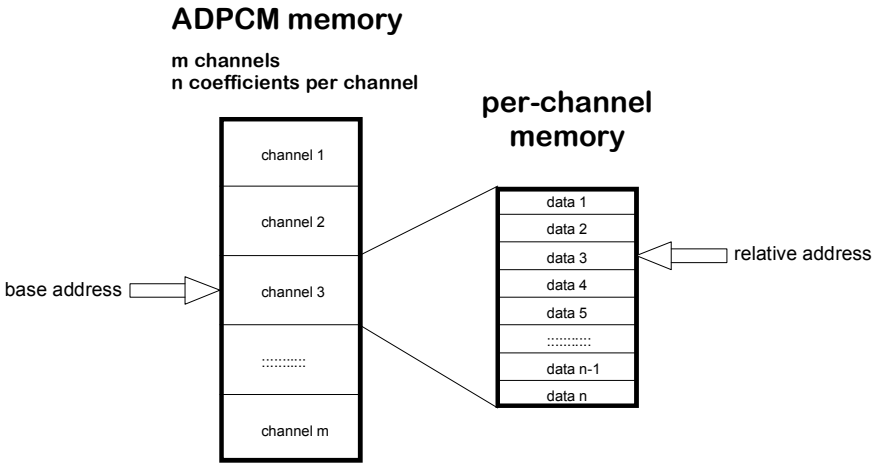
The interface unit acts as the interface of the ADPCM encoder/decoder and its environment. Currently there are two implementations of this interface available. One simple serial interface as used by popular ADPCM stand-alone devices (Sierra's SC11362 or NSC's TP11362) and one simple parallel interface. Due to this structure it is easy to adapt the interface without changing the ADPCM computational unit.



ADPCM top level circuit diagram

The ADPCM core unit performs all computations required for the encoding or decoding operation of the current channel. All data is stored in two RAMs that are hold in the memory unit. This memory unit is the only technology dependent circuitry of the design since memories are usually generated by some kinds of generator software for both ASIC and FPGA technology.

Each channel requires 14x16 bits and 8x11 bits of memory. The memory is addressed using a base address defined by the channel currently processed and a relative address used by the internal state machine.



ADPCM IP core: memory model

It is important to note that only the memory scales linearily with the number of channels to be processed. All other units are more or less fixed in size. Only the interface unit will enlarge with the number of channels *n* by *log* n.

The system clock required for the proper operation of the device may be derived by a simple formula:

$$f_{req} = f_{sample} \cdot 48 \cdot n$$

With f_{sample} is the sampling frequency (usually 8 kHz) and *n* as the number of channels.

For ASIC designs the ADPCM core enables the user to apply straight forward full scan insertion. The generated RAM blocks are encapsulated in a separate module enabling simple BIST insertion for testing these RAMs.

Sample FPGA Implementation

The following table shows the results of some implementation runs of the ADPCM IP core with different configurations on an Altera APEX20kE device.

channels	PCM	LEs	ESBs	f_{req} [MHz]	f_{max} [MHz]	Part
4	law	2819	2	1,54	22,09	EP20K200EBC356-1
8	law	2852	2	3,07	22,35	EP20K200EBC356-1
16	law	2916	3	6,14	22,56	EP20K200EBC356-1
32	law	3038	6	12,28	21,67	EP20K200EBC356-1
64	law	3253	11	24,6	25,0	EP20K200EBC356-1
8	lin	2461	2	3,07	21,33	EP20K200EBC356-1
16	lin	2524	3	6,14	22,24	EP20K200EBC356-1
32	lin	2618	6	12,28	21,2	EP20K200EBC356-1
64	lin	2812	11	24,6	25,0	EP20K200EBC356-1

The ADPCM IP core may be implemented using any other Altera or Xilinx FPGA family that supports the logic density and the required amount of block memory. The next table shows the results of some implementation runs of the ADPCM IP core with different configurations on a Xilinx Virtex-E device.

channels	PCM	LUTs	Block RAMs	f_{req} [MHz]	f_{max} [MHz]	Part
4	law	2518	2	1,54	26,0	XCV400E-8-BG432
8	law	2491	2	3,07	24,9	XCV400E-8-BG432
16	law	2542	2	6,14	24,0	XCV400E-8-BG432
32	law	2612	3	12,28	25,7	XCV400E-8-BG432
64	law	2685	6	24,6	24,6	XCV400E-8-BG432
8	lin	2120	2	3,07	28,0	XCV400E-8-BG432
16	lin	2176	2	6,14	25,2	XCV400E-8-BG432
32	lin	2195	3	12,28	25,2	XCV400E-8-BG432
64	lin	2329	6	24,6	25,4	XCV400E-8-BG432

Licensing

The parametrizeable ADPCM IP core is available either via a source code license or a technology netlist license. There is a complex VHDL testbench setup available to verify the ITU standard compliance of this ADPCM IP core.

More Information

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