GENERAL INFORMATION

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- **Project Start:** January 1st, 2011
- **Project Length:** 2 years
- **FIT-IT Project:** #825904
- **Project Partner:**
  - Oregano Systems Design and Consulting (Austria)
- The project Ætas is sponsored by the Austrian Federal Ministry for Transport, Innovation and Technology under the FIT-IT Programme.

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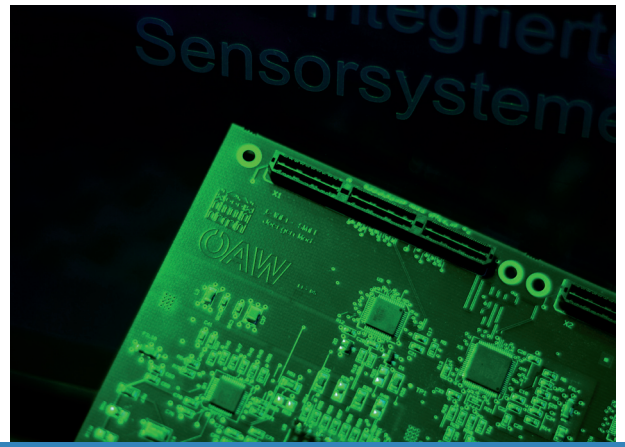
PROJECT OBJECTIVES

High precise clock synchronization is essential in many different areas. Although todays technology already allows rather accurate synchronization (with an accuracy of about 10 ns) for certain applications (measuring pulses that propagate with velocities close to the speed of light) it needs to be even more exact. This is what the FIT-IT Project Ætas aims for.

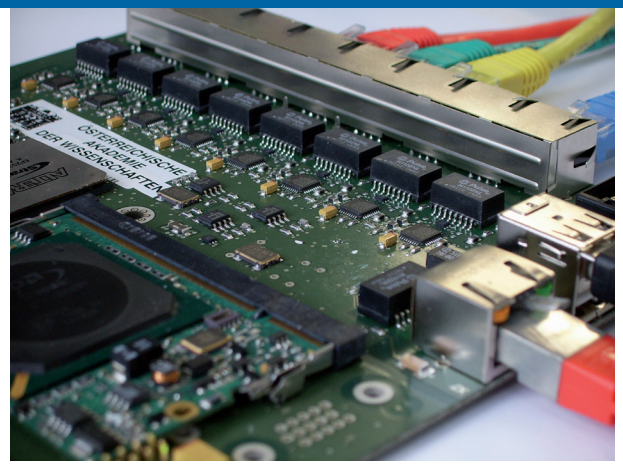
One application area where such a high precise clock synchronization is needed is in wireless position determination (e.g. as in another IISS project ε-WiFi). As the light travels about 30 cm within one nanosecond, one must measure time with a sub-nanosecond accuracy to carry out precise localisations.

Another examplary usecase can be found in CERN. Here, the particle beam has nearly the speed of light and even the slightest deviation of its orbit would have unwanted consequences. Therefore, all parameters have to be changed at exactly the same time and thus be synchronized.

Furthermore, very high accuracy is needed at the stock exchange. Here for example one must be able to tell precisely who was the first to buy a certain share. In critical situations the accuracy of the shareholder's clocks therefore also has to be in a sub-nanosecond range.



PROJECT DESCRIPTION



The goal of Ætas (Advanced Ethernet for Time-aware Syntonicity) is to reach clock synchronization with an accuracy of about 100 ps. Hence, different changes have to be applied to the current method used for synchronization.

Hardware-only Clock Synchronization

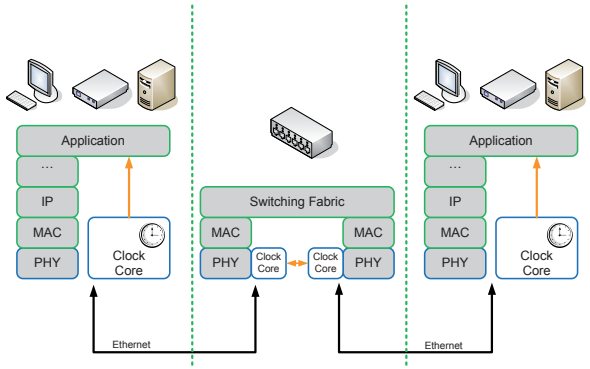
At the moment, clock synchronization is spread over several different communication layers. This, however limits the accuracy of the synchronization, as it is nearly impossible to tell how long the communication between the layers takes, as the needed time is always fluctuating.

For this reason the idea arose to carry out the whole clock synchronization in the physical layer only, by using the special Ætas Physical Layer Device (PHY). This radical technical approach opens a market niche for on the one hand cheap and on the other hand highly accurate clock synchronization transparent to the user application.

PROJECT DESCRIPTION

Solving Asymmetry

One of the biggest problems in clock synchronization schemes is the asymmetry, affecting the achievable accuracy. Different lengths of the cable pairs used for transmitting and receiving data contribute to the offset between clocks. Thus, high accuracy can be reached by using the same cable pair for both directions.
Furthermore, as the synchronization data is embedded into an additional low bandwidth data channel on the physical layer, it is not at all affecting the standard data transmission.



Project Goal

The envisioned solution will keep the system synchronization using the Ætas PHY as easy as plugging the devices together. The initial startup phase will lead to automatic and, due to the lack of asymmetry, enhanced synchronization of slaves to the master, making the concept attractive for small embedded systems, limited in memory and processing power.