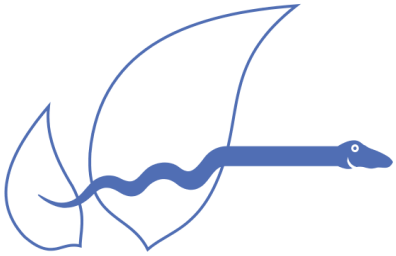

syn1588 ®

PCI Express Ethernet Network Interface Card – Revision 2.1

syn1588® PCIe NIC

Data Sheet

Version 3.1 – Mai 27th 2019

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0 Legals

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1 Overview

1.1 Functional description

The syn1588® PCIe NIC is a 10/100/1000 Mbit Ethernet network interface card (1-lane PCI Express low-profile card) with enhancements to provide the network node with accurate clock synchronization via Ethernet following the IEEE1588 standard.

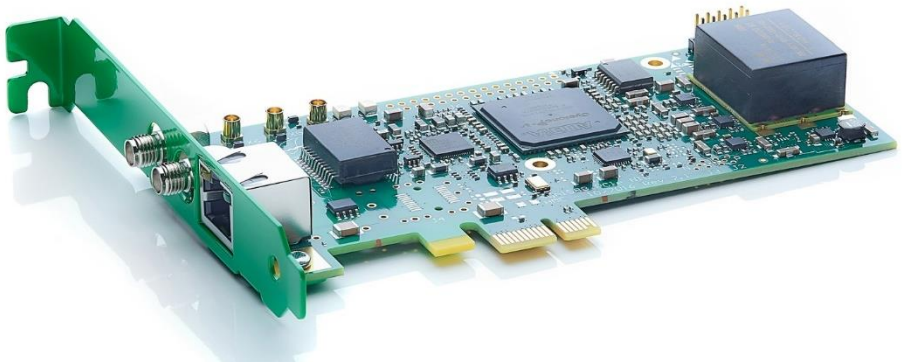

Figure 1: syn1588® PCIe NIC – Revision 2.1

The syn1588® PCIe NIC is using the Oregano Systems syn1588® technology for time stamping of arbitrary network packets. The timestamping unit is fully user configurable enabling any type of packet timing application. The syn1588® PCIe NIC provides full support for IEEE1588-2002 as well as IEEE1588-2008 specific features like the patented on-the-fly timestamping mechanism (one-step mode).

2 Features

The following features are based on the hardware build ID 749 of the syn1588® PCIe NIC – Revision 2. Other build versions of the syn1588® PCIe NIC will offer somewhat different capabilities. Please contact Oregano Systems support for details.

2.1 NIC Features

- Standard 10/100/1000 Mbps Ethernet network card following IEEE802.3-2005
- Green Ethernet (EEE Energy Efficient Ethernet) following IEEE802.3az
- 1-lane PCI Express (PCIe) low-profile card
- Compliant to PCI Express version 2.0 (5 Gbit/s)
- Compatible with PCI Express version 1.1 (2.5 Gbit/s)
- Supporting 10/100/1000 Mbit operation (copper modes, RJ45 connector)
- Automatic cross-over detection function (MDI/MDI-X)
- Optional 1000BASE-X fibre version available (SFP type)
- 4 kByte Ethernet transmit FIFO buffer, 8 kByte Ethernet receive FIFO buffer
- VLAN and IPv6 support
- Promiscuous mode supported
- Up to four user programmable SMA connectors
- Driver software available for Linux and Windows. Both 32 bit and 64 bit systems are supported.

2.2 IEEE1588 Features[1]

- Fully IEEE1588-2002 and IEEE1588-2008 compliant
- Support for Oregano Systems' patented syn1588® technology:
- On-the-fly timestamping while sending or receiving time sync packets (1-step mode)
- IEEE1588 hardware clock - the IEEE1588 clock is fully maintained in hardware
- Clock servo operation is controlled by the software without real-time requirements
- IEEE1588 hardware clock utilizes IEEE1588 time format
- Software does not need to run time format conversions

[1] Requires the Oregano Systems syn1588® PTP Stack to run the protocol engine.

- syn1588® clock frequency is 125 MHz
- All real-time functions for IEEE1588 are implemented in hardware eliminating real-time constraints for the syn1588® PTP Stack
- IEEE1588 master and slave operation supported[2]
- High quality TCXO oscillator (better than 1.5 ppm)
- Optional high-stability OCXO oscillator (better than 0.5ppm)
- Optional clock input to drive the syn1588® clock
  3V3 level, SMA, selected clock frequencies
  (new with revision 2.1)
- 1 PPS output signal[3]
- One pulse per second, rising edge, if seconds wrap in the IEEE1588 hardware clock
- Programmable interrupt conditions
- Up to four programmable input/output signals available on SMA connectors (50 Ω, 3V3 LVCMOS signal levels):
- 1PPS input and/or output
- Up to two EVENT inputs
- Up to two TRIGGER outputs
- Up to two PERIOD outputs
- IRIG-B007 output data stream generation
  (DCLS signal, no carrier, BCD + BCD_Year + SBS)
- Optional IRIG-B007 input decoding
  (DCLS signal, no carrier, BCD + BCD_Year)
- On-board jitter cleaner PLL for generating accurate, synchronized single-ended frequencies up to 156.25 MHz
- Connectivity to an external GPS receiver via the 1 PPS input as well as a serial port of the host PC for external synchronization
- Serial port not included in the syn1588® PCIe NIC, NMEA-0183 RMC messages required
- Binary run-time license for syn1588® PTP Stack included
- Several utilities are available for accessing registers, synchronizing the node's system clock, or synchronizing to an external GPS receiver.

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[2] Oregano Systems generally recommends using the OCXO option for all master applications.

[3] Constant delay of three clock periods to the external output signal. Minimum pulse width is 100 µs.

- Software APIs are available allowing the user to write custom software including interrupt service routines accessing the syn1588® functions, accessing all hardware clock related functions and controlling/observing the syn1588® PTP Stack
- syn1588® Linux Live System for fast testing of the syn1588® PCIe NIC without the need of software installation. Just install the syn1588® PCIe NIC in your node and boot the PC using the syn1588® Linux Live System

2.2.1 Timestamping

- Programmable timestamping unit on Ethernet receive and transmit path for time stamping IEEE1588 packets
- Independent timestamp FIFOs for Ethernet receive path (256 words) and Ethernet transmit path (16 words) allows timestamping of multiple dense packets without losing data thus removing the software real-time requirements
- Patented on-the-fly timestamping for 1-step operation on Ethernet transmit path
- 1-step timestamping just supported for 100 Mbit and 1000 Mbit full duplex operation
- Timestamping supported for VLAN as well as IPv6 operation
- Timestamping of two external input signals – EVENT: On the rising edge of these external signals a timestamp will be drawn
- For EVENT0 input a 16 entry timestamp FIFO is implemented allowing timestamping of dense events with a distance of just 100 ns
- Extremely high timestamp resolution of 5 ns

2.2.2 User Programmable Events

- TRIGGER: Two user programmable single event output signals may be generated
- These TRIGGER signals change their respective state at a programmable time that is derived from the highly accuracy IEEE1588 hardware clock
- TRIGGER0 output is controlled by a 16 entry FIFO providing support for dense event sequences without imposing real-time requirements on the software
- Resolution of all TRIGGER events is +/-5 ns
- Maximum TRIGGER event duration is 32 bit seconds
- PERIOD: Two user programmable periodical output signals may be generated that are derived from the highly accuracy IEEE1588 hardware clock
- The frequency may be selected in the range of mHz to 156.25 MHz
- The resolution of all PERIOD events is 2^{-16} ns, i.e. 0,0153 ps
- The maximum PERIOD duration is 65535 seconds (16 bit)

2.3 Hardware Options

- High precision OCXO (0.05 ppm) for master operations or high accuracy applications.
- SFP option: fibre interface 1000BASE-X using SFP type interface

3 Block Diagram

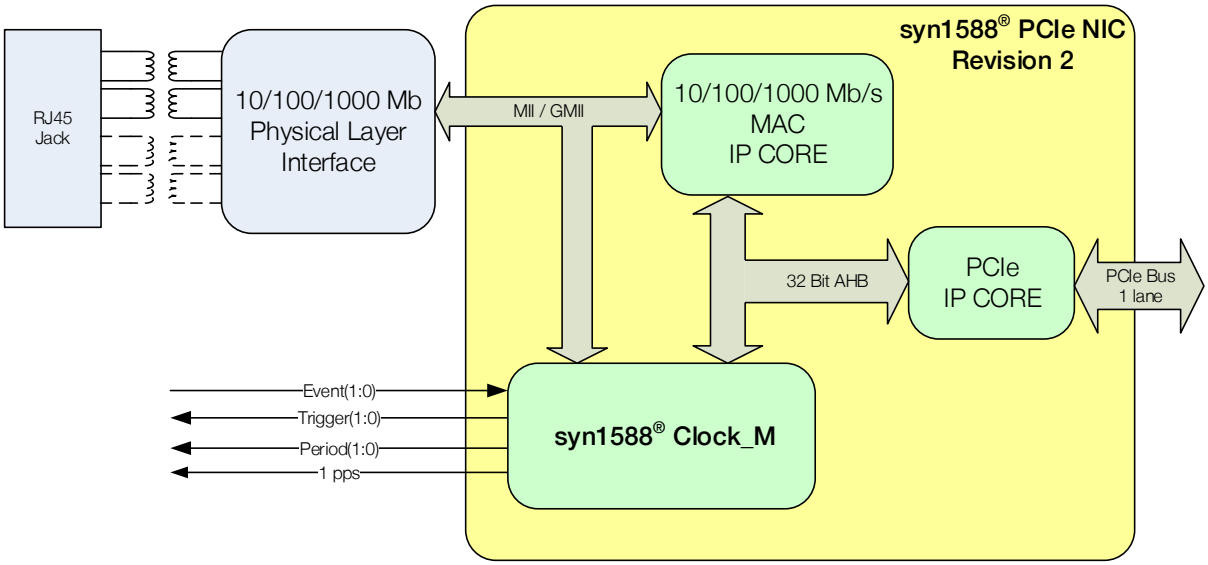

Figure 2: syn1588® PCIe NIC: block diagram

The syn1588® PCIe NIC basically consists of a single FPGA containing the following IP cores:

- 10/100/1000 Mbps Ethernet Media Access Controller (MAC)
- syn1588® Clock_M IP Core
- PCIe interface

4 Mechanics

The following figure shows the dimensions of the syn1588® PCIe NIC board revision 2.0.

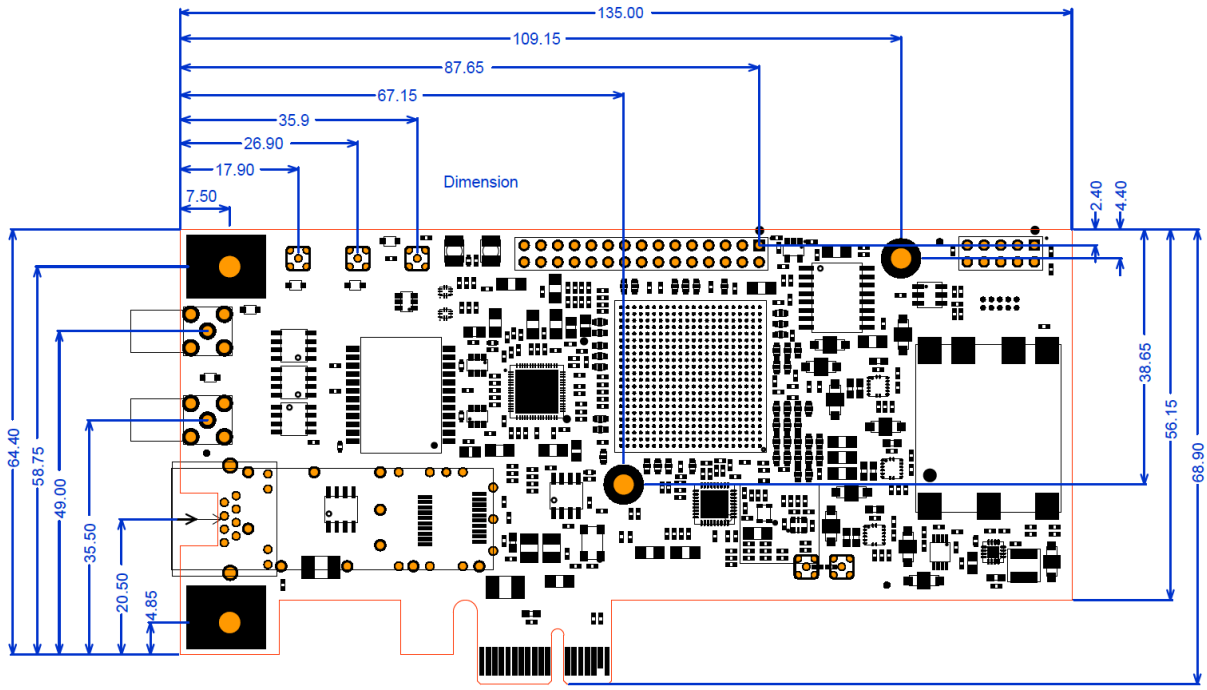

Figure 3: syn1588® PCIe NIC – Revision 2.1: dimensions & placement of connectors

Please note that the position of the connectors did not change with respect to the previous revision 1.5 and 2.0 of the syn1588® PCIe NIC.

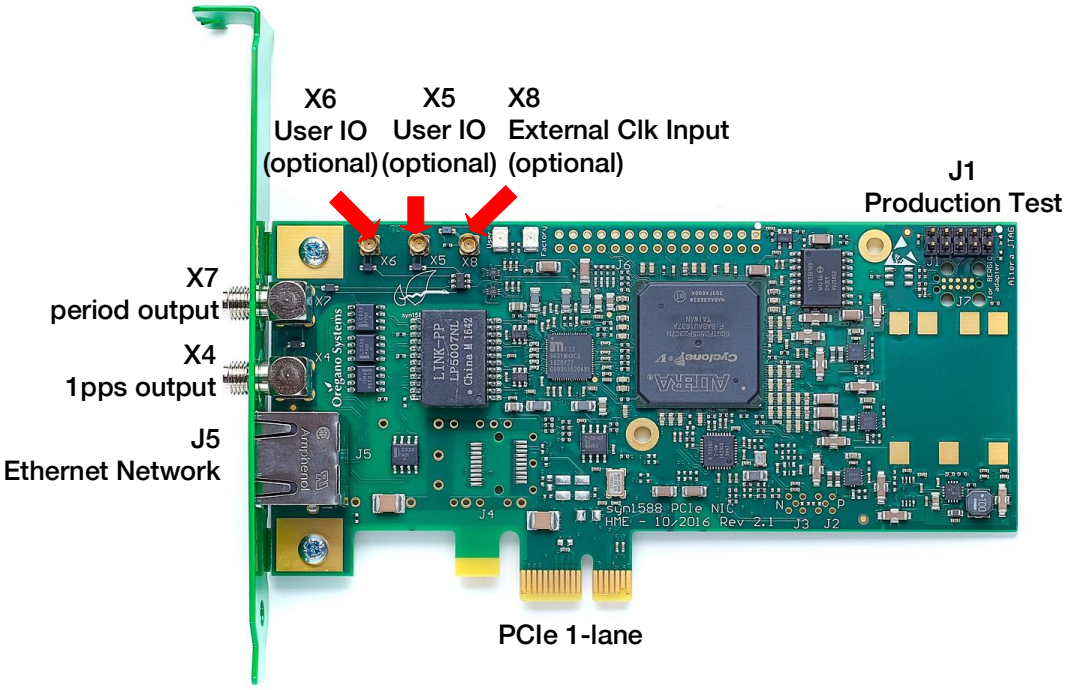

Figure 4: syn1588® PCIe NIC Revision 2.1: connectors

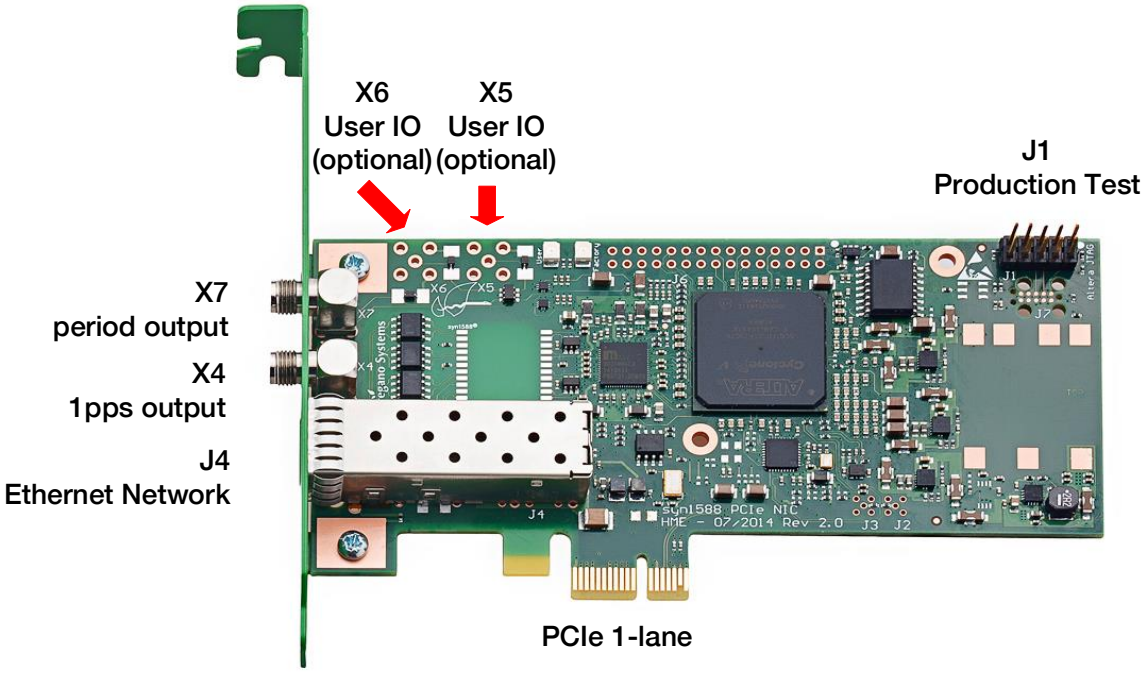

Figure 5: syn1588® PCIe NIC Revision 2: connectors for SFP version

Oregano Systems offers two different types of brackets for the syn1588® PCIe NIC to facilitate any type of mounting situation:

- Low-profile bracket with 2 SMA connectors (default option)
- Standard bracket with 2 SMA connectors

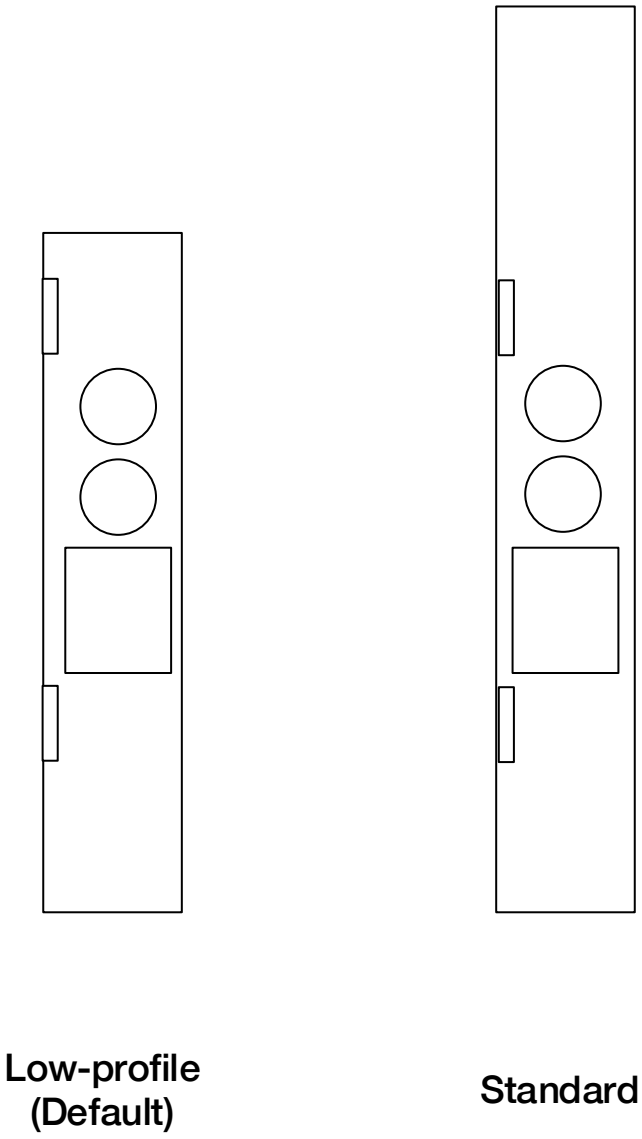

Figure 6: syn1588® PCIe NIC: PCI bracket options

5 Electrical Interface Specification

5.1 ESD

All user accessible connectors of the syn1588® PCIe NIC are protected against ESD damage following IEC61000-4-2 15 kV air 8 kV contact. The copper Ethernet interface X1 is additionally protected against lightning following IEC61000-4-4 40 A (5/50 µs) and IEC61000-4-5 95 A (8/20 µs) as well as Bellcore 1089 (intra-building) 100 A (2/20 µs).

5.2 Power Supply

The syn1588® PCIe NIC revision 2.1 board is operated using the 3V3 power supplied by the PCI Express edge connector. The oscillators – the TCXO as well as the optional OCXO - are powered by highly stable on-board supply which uses the 12V supplied by the PCI Express edge connector.

DC Characteristics	
Minimum DC 3V3 input voltage	3.0 V
Maximum DC 3V3 input voltage	3.6 V
Maximum DC supply current @ 3,3 V	1.0 A
Minimum DC 12V input voltage	11.5 V
Maximum DC 12V input voltage	12.5 V
Maximum DC supply current @ 12V	0.2 A

Table 1 Power supply DC characteristics

5.3 Ethernet: Copper (J5)

The Ethernet interface follows IEEE standard 802.3-2005. The syn1588® PCIe NIC Revision 2.1 supports EEE (Energy Efficient Ethernet aka Green Ethernet) following IEEE 802.3az. This function is deactivated by default and can be activated via the software driver.

5.4 SFP Ethernet Interface (J4)

The SFP interface supports just 1000BASE-X mode using the following SFP transceiver modules.

Vendor	Type	Mode	Range	Connector	Order Number
Avago	fibre	1000BASE-X	short (550 m)	LC	AFBR-5710PZ
Avago	fibre	1000BASE-X	long (10 km)	LC	AFCT-5710PZ
Fiberstore	fibre	1000BASE-X	short (550 m)	LC	SFP1G-SX-85
Fiberstore	fibre	1000BASE-X	long (10 km)	LC	SFP1G-LX-31
Teosco	fibre	1000BASE-X	short (550 m)	LC	TEO-1.25GSFP-02
Teosco	fibre	1000BASE-X	long (10 km)	LC	TEO-1.25GSFP-10
Finisar	fibre	1000BASE-X	short (550 m)	LC	FTRJ-8519
Finisar	fibre	1000BASE-X	long (10 km)	LC	FTLF1318

Table 2 Supported SFP transceiver modules

5.5 User Interface (X4 – X7)

There are four SMA connectors available for the user. Two input and two output signals.

- X4: 1 PPS / period output signal
- X7: trigger output signal
- X6: event input signal
- X5: 1 PPS input signal

The output signals deliver a standard 3V3 level 50 Ω output signal driving a maximum of 20 mA. The input signals expect a standard 3V3 level signal. The output signals may drive two or three standard loads when using correct 50 Ω cabling.

Two SMA connectors (X4 and X7) are directly available at the PCI bracket while two more connectors (X5 and X6) are available internally. Starting with board revision 2.1 the internal connectors are of MMCX type. Upon request (via the appropriate ordering code) Oregano Systems supplies the cable to directly connect to a SMA port.

5.5.1 SMA Output Characteristics

Output coupling	DC
Output threshold high	2.8 V min
Output threshold low	0.4 V max
Absolute maximum applied voltage	-0 V to 3.465 V
Output to output skew, synchronous	< 1 ns typical
Output current	±20 mA max

Table 3 SMA Output Characteristics

5.5.2 SMA Input Characteristics

Input impedance	50 Ω nominal
Input coupling	DC
Voltage level	0 to 3.3 V
Absolute maximum input voltage	-0.5 V to 4.25 V
Minimum pulse width	500 ns
Input threshold high	2.0 V
Input threshold low	0.8 V

Table 4 SMA Input Characteristics

5.6 External clock Input Interface (X8)

Optionally there is an external clock input available to allow direct driving the syn1588® hardware clock from this external signal.

Input impedance	50 Ω nominal
Input coupling	DC
Voltage level	0 to 3.3 V
Absolute maximum input voltage	-0.5 V to 4.25 V
Input threshold high	2.0 V
Input threshold low	0.8 V

Table 5 External Clock Input Characteristics

5.7 Production Test (J1)

The production test connector must be left unconnected while the syn1588® PCIe NIC is operated. Note that there is no special ESD protection for this interface.

6 Environmental

6.1 Temperature

Operating temperature range 0° C ... +50° C

Storage temperature range -40° C ... +85° C

6.2 Humidity

Operating humidity 5% to 80% RH, non-condensing

6.3 Weight

Total weight approx. 70 g (without OCXO)

Total weight approx. 75 g (with OCXO)

7 Installing the syn1588® PCIe NIC Hardware

The following instructions are general installation guide lines. Consult your computer's user manual for specific instructions and warnings for installing new PCI/PCIe components.

Caution

The syn1588® PCIe NIC is sensitive to electrostatic discharge that may damage the unit. Please observe ESD protection rules. Do not directly touch the unmounted syn1588® PCIe NIC while not being properly grounded. Use the ESD bags provided by Oregano Systems for shipping and storage.

7.1 Installation

- Be sure to have powered–off your PC prior to installing the syn1588® PCIe NIC. Failure to do so could endanger you and may damage the syn1588® PCIe NIC or computer

- Please be sure to thoroughly ground yourself by means of a grounding strap or by touching a grounded object prior to unpacking the syn1588® PCIe NIC card

- Insert the syn1588® PCIe NIC into the empty PCIe slot and verify that the card is properly inserted and fastened by means of levels or screw of the case

- Plug in the power cord of the computer and power the computer on

The syn1588® PCIe NIC card is now installed.

Caution

Please note that some BIOS implementations do not allow plugging a 1-lane PCIe card into an 8-lane or 16-lane slot. Please consult your BIOS manual in case of troubles.

8 Software

8.1 Driver

The syn1588® PCIe NIC requires a driver software for its operation on your host PC. There are drivers available for Linux and Windows for both 32 bit and 64 bit systems. Currently, the following operating systems are officially supported.

OS
Windows XP
Windows 7 (x32/x64)
Windows 8 (x32/x64)
Windows 10 (x32/x64)
Windows Server 2003 (x32/x64)
Windows Server 2008 (x32/x64)
Windows Server 2012 (x32/x64)
Linux kernel version 2.6.16 – 4.10.0

Table 6 Driver software: supported OS

Please consult the syn1588® User Guide for further installation instructions.

Please be aware that the current driver versions do not support any power-saving mode like stand-by or hibernation. The syn1588® PCIe NIC needs to be restarted by reloading the driver.

8.2 syn1588® PTP Stack

Every syn1588® PCIe NIC comes with a binary run-time license of the syn1588® PTP Stack. The syn1588® PTP Stack is available for both Windows and Linux. The syn1588® PTP Stack supports all operating system versions listed in Table 6 Driver software: supported OS

Please refer to the syn1588® User Guide for more information on using syn1588® software.

9 Further Information

You are looking for further information not included in this datasheet? Please contact Oregano Systems support! We will be pleased to provide you all the required information.

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Wien, January 10th 2017

Certificate of Conformance

The Oregano Systems Ethernet network interface card with IEEE1588 capabilities "syn1588® PCIe NIC" (board revision 1.5) meets the intent of .Electromagnetic Compatibility directive 2004/108/EC, Low Voltage directive 2006/95/EC and safety requirements for electrical equipment for measurement, control and laboratory use.

Compliance was demonstrated to the following specifications:

- EN55022:2010
- EN55024:2010
- EN/IEC60950-1:2005 (2nd Edition)+A1:2009

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RoHS Certificate of Conformance

The Oregano Systems' syn1588® products listed below is (are) in compliance with Directive 2011/65/EC on the restriction of the use of certain hazardous substances in electrical and electronic equipment (RoHS Directives).

- syn1588® Gbit Switch (board revision 1.7)
- syn1588® PCIe NIC (board revision 1.5)
- syn1588® PCIe NIC Revision 2 (board revision 2.0)
- syn1588® PCIe NIC Revision 2.1 (board revision 2.1)
- syn1588® VIP Evaluation Board (board revision 2.1)

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Wien, January 10th 2017

Letter of Volatility

The following table shows the non-volatile memories of the syn1588® PCIe NIC – Revision 2.1. Please note that no customer data is stored in these non-volatile memories.

memory	function	size	writeable	user R/W	access restriction
SPI Flash U17 Micron N25Q128A13ESF40G	FPGA configuration storage	128Mbit	yes	no	dedicated firmware update software required, only user configuration may be written, factory default configuration is write protected in hardware
I2C EEPROM U1 ON Semiconductor CAT24AA01TD	MAC address	1kbit	no	no	no write access implemented in hardware

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