Version 1.4 – January 2020

Abstract

This application note describes how to use the video add-on function available for the syn1588® PCIe NIC.

Introduction

The syn1588® PCIe NIC is optionally equipped with a video add-on board that allows generation of analog video sync signals. Ordering code is SYN1588PCI-Video. Lease see application note: “Ordering syn1588® PCIe NIC Revision 2.1” (AN002, Version 2.8 - March 2019) for details. This application note describes in detail how these video sync signals can be generated.

Pre-Requisites

The following requirements have to be met in order to generate video sync signals using the syn1588® PCIe NIC with the video add-on option:

Figure 1 syn1588® PCIe NIC with the video add-on option

- syn1588® PCIe NIC with the video add-on
- driver software for the syn1588® PCIe NIC
- syn1588® PTP Stack
- vSync utility
- Administrator rights to run the syn1588® software

All software may be found on the wooden syn1588® USB stick that comes with every syn1588® PCIe NIC.

Figure 2 syn1588® USB stick

Optionally, the software can be downloaded from the Oregano Systems secure file server. Please contact Oregano Systems support (support@oregano.at) in order to receive an account for this secure file server.

The vSync Utility

There is a dedicated utility vSync that controls the generation of the video sync signals. The following listing shows the usage screen of vSync:

```
root@ubuntu:/opt/oregano# ./vsync -h
syn1588(R) vSync - Video Synchronization Engine
Build date: Apr 24 2017 - V 1.4-16 Rev g7660339
Copyright (c) Oregano Systems - Design & Consulting GesmbH 2005-2017
Confidential unpublished data - All rights reserved

Command line: ./vsync -h
usage: vsync [-h][-d card][-I clockID][-f filename][-d card][-m
videoMode] [-o ptpPort][-t Timing][-c offsetCompensate][-v logLevel]

-h              shows this usage screen
-d card         select the device driver (syn1588 card number) [0]
-f filename     use the file 'filename' for logging [stdout]
-m videoMode    select the desired video mode. disabled by default[0]
                    525i     ST170 NTSC interlaced (525i 30/1001 Hz)
                    625i     ST170 PAL  interlaced (625i 25 Hz)
                    720p50   ST296 progressive     (720p 50 Hz)
                    720p59   ST274 progressive     (720p 60/1001 Hz)
                    1080i50  ST274 interlaced      (1080i 50 Hz)
                    1080i59  ST274 interlaced      (1080i 60/1001 Hz)
                    1080p50  ST274 progressive     (1080p 50 Hz)
                             not-supported by DAC, digital only
                    1080p59  ST274 progressive     (1080p 60/1001 Hz)
                             not-supported by DAC, digital only
-o ptpPort      set the ptp port number for shared memory access [1]
-t Timing       select if DAC is used or only digital
                sync signals used [DAC]
                    DAC   - output Timing for the Video DAC Add-on board
                    digital - output Timing for digital sync signals
-c offsetCompensate    set offset to adjust in 15-bit nanoseconds [0]
selectable range (-32768 ns to 32767 ns)
-I clockID      specify clock identity for configuring boundary clock [0]
-v logLevel     change verbosity level (0..4)[0]
```

Quick Start: Generating an Analog Video Sync Signal

Step 1; Identify your syn1588® PCIe NIC

Open a syn1588® shell and start the syn1588® utility by using the command "./syn1588". In our example we just have one syn1588® PCIe NIC. If you have more than one syn1588® PCIe NICs in your system type the command "listcards" to identify your syn1588® PCIe NIC with mounted video adapter board.

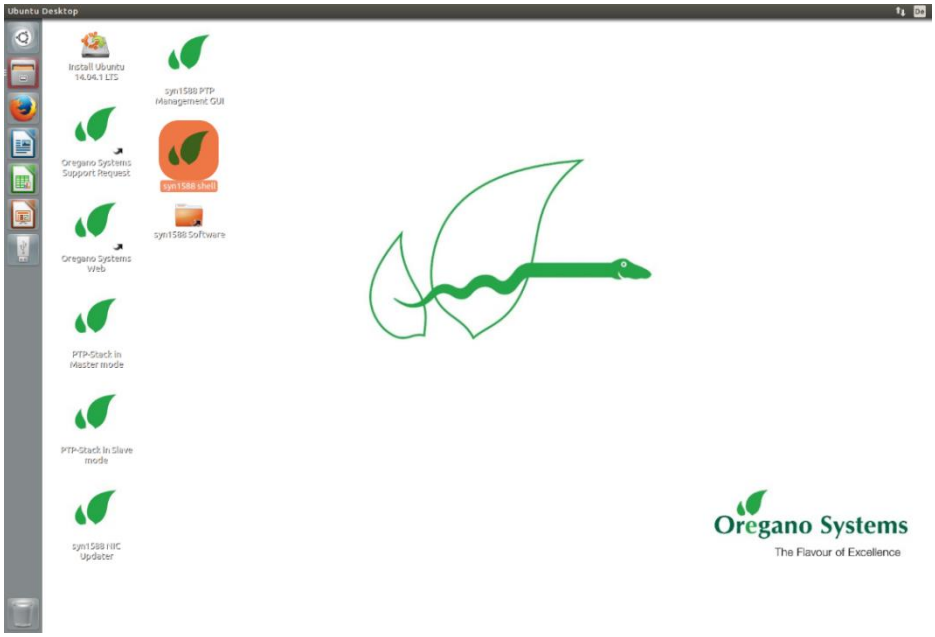

Figure 3 Open syn1588 shell

```
root@ubuntu:/opt/oregano# ./syn1588
syn1588(R) Driver Interface - V 1.3.3 Rev 1221 - Dec  1 2016
Copyright (c) Oregano Systems - Design & Consulting GesmbH 2005-2015
Confidential unpublished data - All rights reserved

Syn1588Ifc: Device /dev/syncD0 found
syn1588(R) Hardware Clock M 2.3.2 f=125000000 Hz
Selected syn1588(R) card 0
>listcards

card 0 is 8c:a5:a1:ff:fe:00:00:6b
>quit
root@ubuntu:/opt/oregano#
```

After identifying your card number quit the syn1588 utility by using the "quit" command. Use command "ifconfig" to find out the Ethernet interface of your syn1588® PCIe NIC by comparing the MAC addresses. In our example it is "eth1".

Caution:

Do not invoke the syn1588 utility after starting the vSync utility as the former initializes the Jitter Cleaner PLL which causes the PLL to loose lock. One may start the syn1588 utility in a separate shell and keep it open for purposes like re-configuring the IOMATRIX register, etc.

```
root@ubuntu:/opt/oregano# ifconfig
eth0      Link encap:Ethernet  HWaddr d0:50:99:2a:ef:05
          inet addr:192.168.102.192  Bcast:192.168.103.255
          inet6 addr: fe80::d250:99ff:fe2a:ef05/64 Scope:Link
          UP BROADCAST RUNNING MULTICAST  MTU:1500  Metric:1
          RX packets:18962 errors:0 dropped:0 overruns:0 frame:0
          TX packets:115 errors:0 dropped:0 overruns:0 carrier:0
          collisions:0 txqueuelen:1000
          RX bytes:3203506 (3.2 MB)  TX bytes:16051 (16.0 KB)

eth1      Link encap:Ethernet  HWaddr 8c:a5:a1:00:00:6b
          inet6 addr: fe80::8ea5:a1ff:fe00:6b/64 Scope:Link
          UP BROADCAST RUNNING MULTICAST  MTU:1500  Metric:1
          RX packets:5235 errors:0 dropped:0 overruns:0 frame:0
          TX packets:875 errors:0 dropped:0 overruns:0 carrier:63
          collisions:0 txqueuelen:1000
          RX bytes:471150 (471.1 KB)  TX bytes:13371102 (13.3 MB)
          Interrupt:16 Memory:90700000-90710000

lo        Link encap:Local Loopback
          inet addr:127.0.0.1  Mask:255.0.0.0
          inet6 addr: ::1/128 Scope:Host
          UP LOOPBACK RUNNING  MTU:65536  Metric:1
          RX packets:163 errors:0 dropped:0 overruns:0 frame:0
          TX packets:163 errors:0 dropped:0 overruns:0 carrier:0
          collisions:0 txqueuelen:0
          RX bytes:11774 (11.7 KB)  TX bytes:11774 (11.7 KB)
```

Step 2: Start syn1588® PTP Stack

Open a syn1588® shell and start the syn1588® PTP Stack by using the command "./ptp". Add the parameters "-i eth1" (interface identified in Step 1), "-C M_EXT" (Master on external reference), "-d 0" (Domain 0..255, default Domain is 0) and optional "-v 2" (loglevel 2 includes errors and warnings).

Alternatively if you want to run the syn1588® PTP Stack in other configuration for example as slave please choose one of your appreciated parameter:

-C options set Clock Class (0..255)

M_EXT....Master on external reference

M_HOLD...Master on external reference (in holdover)

M_NSYNC..Master on external reference (not sync'd)

M_SLAVE..Master on external reference (may be Slave)

S...Slave only

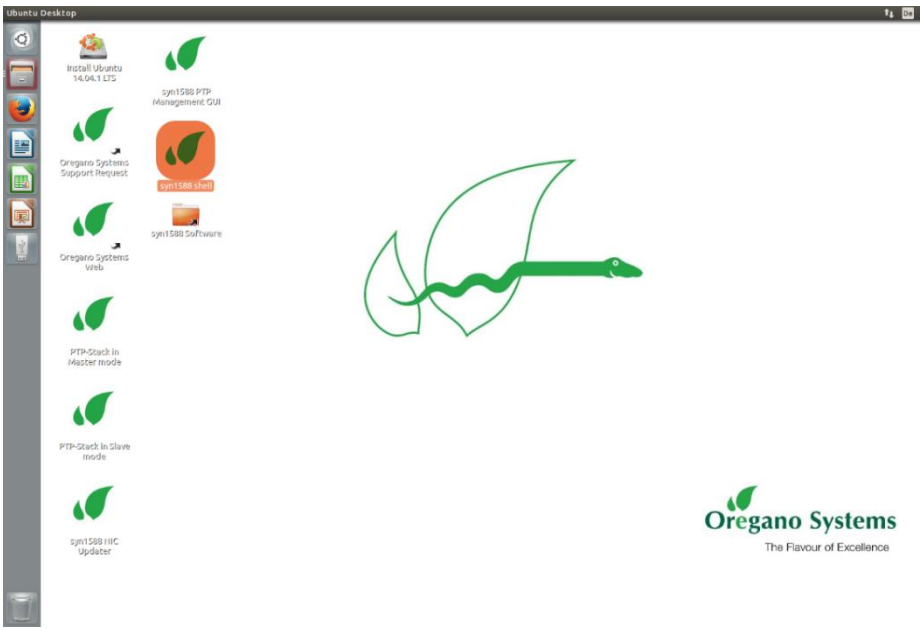

Figure 4 Open syn1588 shell

```
root@ubuntu:/opt/oregano# ./ptp -i eth1 -C M_EXT -d 0 -v 2
syn1588(R) PTP Stack - IEEE1588-2008 Engine
Build date: Apr 24 2017 - V 1.4-16 Rev g7660339
Copyright (c) Oregano Systems - Design & Consulting GesmbH 2005-2017
Confidential unpublished data - All rights reserved

syn1588(R) PTP Stack started: 2017-05-12 09:56:01.772743 (UTC)
Using command line parser.
Port 1: adding config "i" = "eth1"
Port 1: adding config "C" = "M_EXT"
Port 1: adding config "v" = "2"
Port 1: adding config "d" = "10"
Command line: ./ptp_video -i eth1 -CM_EXT -v2 -d10
Found Configuration for 1 ports
(1) Syn1588Ifc: Device /dev/syncD0 found
(1) syn1588(R) Hardware Clock M 2.3.2 f=125000000 Hz
(1) syn1588(R) PCIe NIC, Build 808 with HQ Oscillator
(1) Clk: Using Oregano Systems; syn1588(R) PCIe NIC; 8C:A5:A1:00:00:6B
(1)   with ClockId 8C:A5:A1:FF:FE:00:00:6B
(1) Activated SO_TIMSTAMPING hardware
(1) Activated SO_TIMSTAMPING hardware
(1) Clk: Resetting filters
(1) Init shared mem
(1) syn1588HwClk: UTC offset changed to 37 s
(1) State Change Initializing -> Listening
(1) State Change Listening -> Master
```

Step 3: Start vSync utility with analog mode

Open a syn1588® shell and start the syn1588® vSync utility by using the command "./vsync". Add the command line parameters "-d 0" (card number identified in step 1), choose the selected video mode using "-m 625i" (for this example the video mode ST170 PAL interlaced, 625i, 25Hz is used) and optionally define a verbosity level for the output by "-v 2" (loglevel 2 includes errors and warnings). One can also redirect the log output to a file using the "-f filename" command line option.

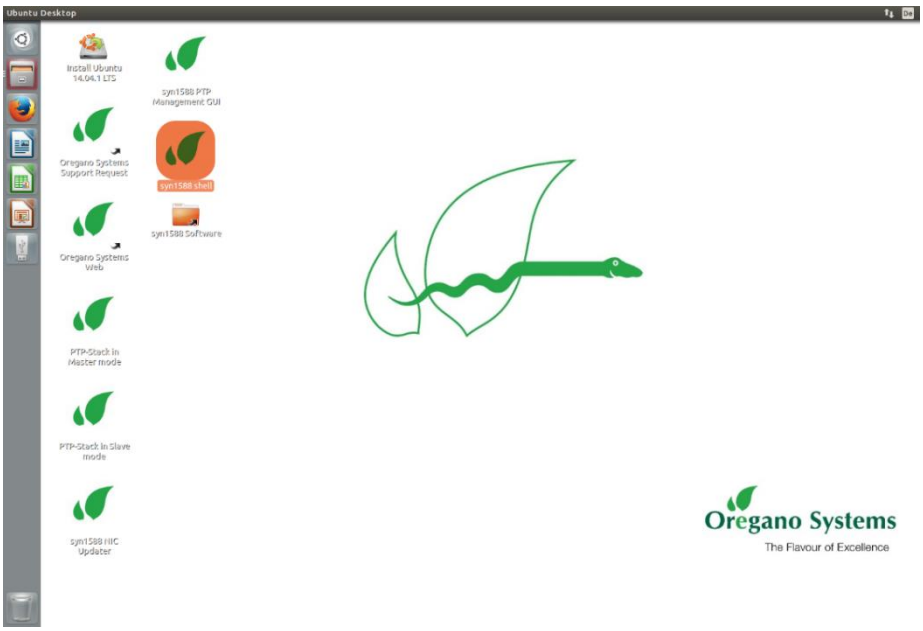

Figure 5 Open syn1588 shell

```
root@ubuntu:/opt/oregano# ./vsync -d 0 -m 625i -v 2
syn1588(R) vSync - Video Synchronization Engine
Build date: Apr 24 2017 - V 1.4-16 Rev g7660339
Copyright (c) Oregano Systems - Design & Consulting GesmbH 2005-2017
Confidential unpublished data - All rights reserved

Command line: ./vsync -d0 -m625i -v2
syn1588(R) PCIe NIC, Build 808 with HQ Oscillator
Opening Shared Memory...
Associated PTP instance: 8ca5a1ffff00006b_001
Video Processing started
Trying to enable pll with frequency: 27000000
sPLLCfgName: 27000000
tPLL.tUpdatePLLCfg: 0
tPll.GetInputFreqPeriodSettings: 62500,0
access_pll: 0
PLL is configured
Register: Addr: 130, Data: 01
PLL is locked
DAC output is enable
```

Figure 6 Analog Video Mode 625i (master operation)

Figure 6 shows the video output (channel 1 / yellow) for the analog video Mode ST170 PAL interlaced, 625i 25Hz and the 1 PPS signal from the syn1588® PCIe NIC (channel 2 / red). The video signal is now perfectly phase locked to the 1 PPS master reference signal. One can use the oscilloscope or any video test equipment to verify this behavior.

Note:

For better understanding of the video output signal, the figure above has been generated with a test-version of the syn1588® PCIe NIC, where not all video-data-bits have been set to zero. In the production version, the data-bits are all set to zero, which generates the so-called “Genlock” signal. But then there would be no visible difference between video signal and blank signal in the figure, except the doubled HSYNC pulse frequency during V-blank.

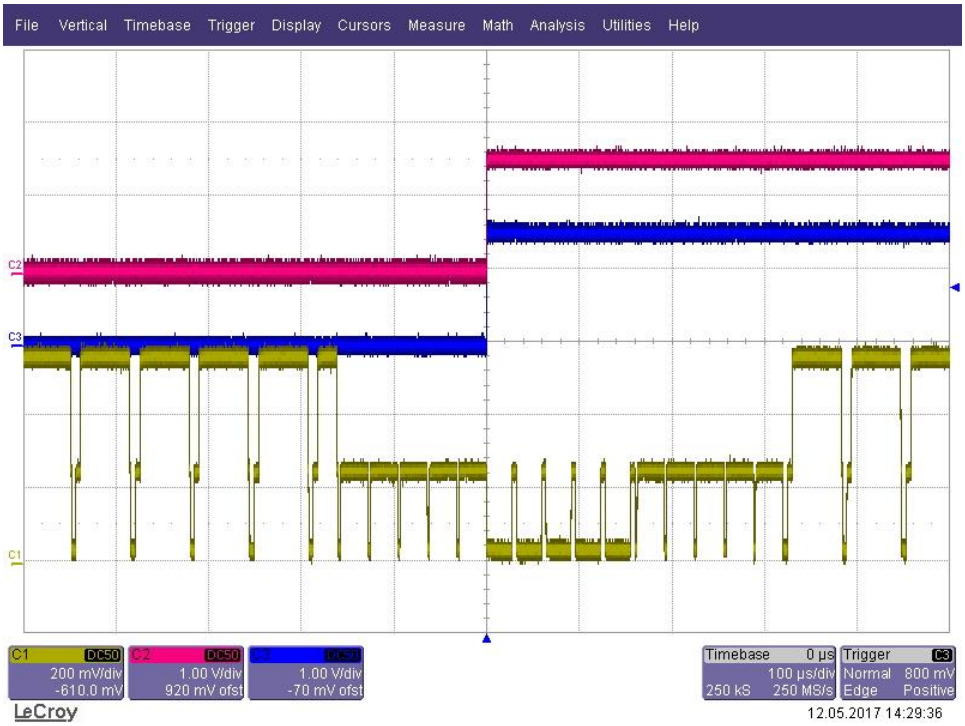

Figure 7 Analog Video Mode 625i (slave operation)

Figure 7 shows the video output (channel 1 / yellow) for the analog videoMode 625i (ST170 PAL interlaced, 25Hz), the 1 PPS signal from the syn1588® PCIe NIC (channel 2 / red) and the 1 PPS signal from the master reference clock (channel 3 / blue). The syn1588® PCIe NIC now acts as slave and is synchronized to an external reference master. The video signal is phase locked to the 1 PPS of the Grandmaster in the network. The jitter between the 1PPS Grandmaster signal and the generated video sync signal depends on the clock synchronization accuracy.

Note:

For better understanding of the video output signal, the figure above has been generated with a test-version of the syn1588® PCIe NIC, where not all video-data-bits have been set to zero. In the production version, the data-bits are all set to zero, which generates the so-called “Genlock” signal. But then there would be no visible difference between video signal and blank signal in the figure, except the doubled HSYNC pulse frequency during V-blank.

Quick Start: Generating a Digital Video Sync Signals

Step 1: Identify your syn1588® PCIe NIC

Open a syn1588 shell and start the syn1588 utility by using the command "./syn1588". In our example we just have one syn1588® PCIe NIC. If you have more than one syn1588® PCIe NICs in your system type the command "listcards" to identify your syn1588® PCIe NIC with mounted Video adapter board.

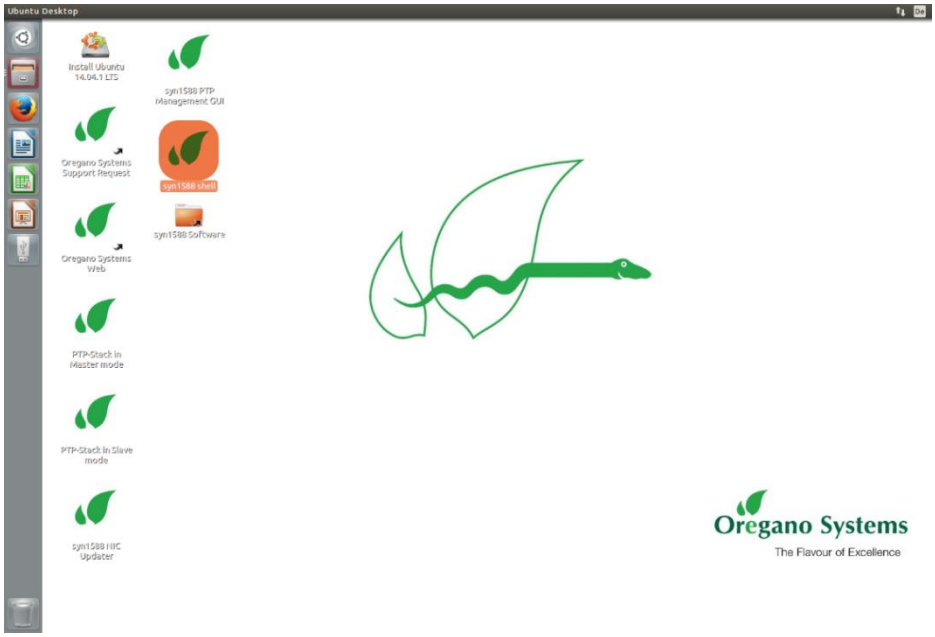

Figure 8 Open syn1588 shell

```
root@ubuntu:/opt/oregano# ./syn1588
syn1588(R) Driver Interface - V 1.3.3 Rev 1221 - Dec  1 2016
Copyright (c) Oregano Systems - Design & Consulting GesmbH 2005-2015
Confidential unpublished data - All rights reserved

Syn1588Ifc: Device /dev/syncD0 found
syn1588(R) Hardware Clock M 2.3.2 f=125000000 Hz
Selected syn1588(R) card 0
>listcards

card 0 is 8c:a5:a1:ff:fe:00:00:6b
>quit
root@ubuntu:/opt/oregano#
```

After identifying your card number quit the syn1588 utility by using the "quit" command. Use command "ifconfig" to find out the Ethernet interface of your syn1588®PCIe NIC by comparing the MAC addresses. In our example it is "eth1".

Caution:

Do not invoke the syn1588 utility after starting the vSync utility as the former initializes the Jitter Cleaner PLL which causes the PLL to loose lock. One may start the syn1588 utility in a separate shell and keep it open for purposes like re-configuring the IOMATRIX register etc.

```
root@ubuntu:/opt/oregano# ifconfig
eth0      Link encap:Ethernet  HWaddr d0:50:99:2a:ef:05
          inet addr:192.168.102.192  Bcast:192.168.103.255
          inet6 addr: fe80::d250:99ff:fe2a:ef05/64 Scope:Link
          UP BROADCAST RUNNING MULTICAST  MTU:1500  Metric:1
          RX packets:18962 errors:0 dropped:0 overruns:0 frame:0
          TX packets:115 errors:0 dropped:0 overruns:0 carrier:0
          collisions:0 txqueuelen:1000
          RX bytes:3203506 (3.2 MB)  TX bytes:16051 (16.0 KB)

eth1      Link encap:Ethernet  HWaddr 8c:a5:a1:00:00:6b
          inet6 addr: fe80::8ea5:a1ff:fe00:6b/64 Scope:Link
          UP BROADCAST RUNNING MULTICAST  MTU:1500  Metric:1
          RX packets:5235 errors:0 dropped:0 overruns:0 frame:0
          TX packets:875 errors:0 dropped:0 overruns:0 carrier:63
          collisions:0 txqueuelen:1000
          RX bytes:471150 (471.1 KB)  TX bytes:13371102 (13.3 MB)
          Interrupt:16 Memory:90700000-90710000

lo        Link encap:Local Loopback
          inet addr:127.0.0.1  Mask:255.0.0.0
          inet6 addr: ::1/128 Scope:Host
          UP LOOPBACK RUNNING  MTU:65536  Metric:1
          RX packets:163 errors:0 dropped:0 overruns:0 frame:0
          TX packets:163 errors:0 dropped:0 overruns:0 carrier:0
          collisions:0 txqueuelen:0
          RX bytes:11774 (11.7 KB)  TX bytes:11774 (11.7 KB)
```

Step 2: Start syn1588® PTP Stack

Open a syn1588 shell and start the syn1588® PTP Stack by using the command "./ptp". Add the parameters "-i eth1" (interface identified in Step 1), "-C M_EXT" (Master on external reference), "-d 0" (Domain 0..255, default Domain is 0) and optional "-v 2" (loglevel 2 includes errors and warnings).

Alternatively if you want to run the syn1588® PTP Stack in other configuration for example as slave please choose one of your appreciated parameter:

-C options set Clock Class (0..255)

M_EXT....Master on external reference

M_HOLD...Master on external reference (in holdover)

M_NSYNC..Master on external reference (not sync'd)

M_SLAVE..Master on external reference (may be Slave)

S...Slave only

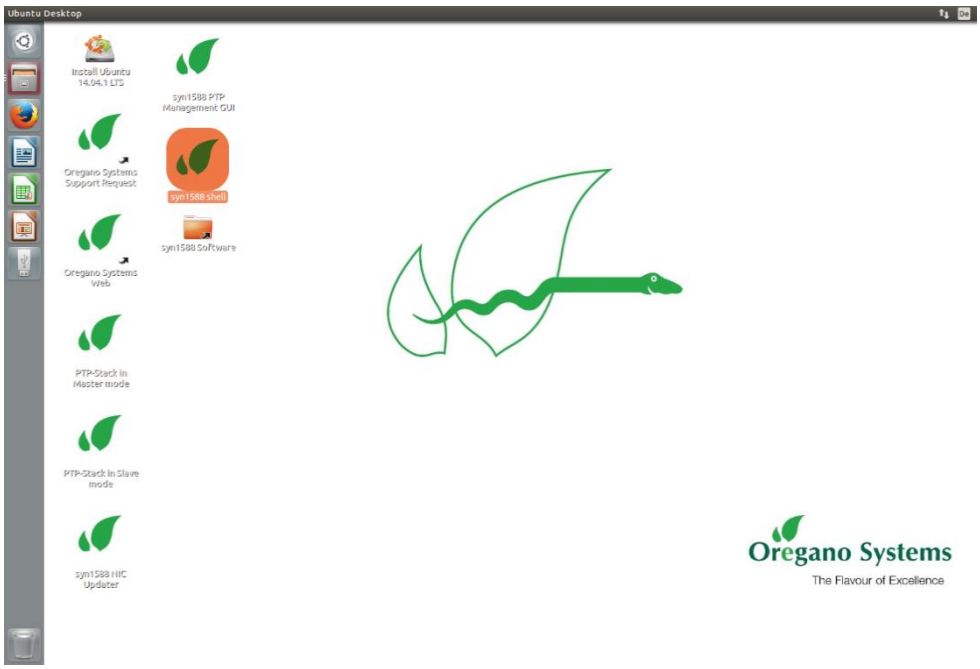

Figure 9 Open syn1588 shell

```
root@ubuntu:/opt/oregano# ./ptp -i eth1 -C M_EXT -d 0 -v 2
syn1588(R) PTP Stack - IEEE1588-2008 Engine
Build date: Apr 24 2017 - V 1.4-16 Rev g7660339
Copyright (c) Oregano Systems - Design & Consulting GesmbH 2005-2017
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syn1588(R) PTP Stack started: 2017-05-12 09:56:01.772743 (UTC)
Using command line parser.
Port 1: adding config "i" = "eth1"
Port 1: adding config "C" = "M_EXT"
Port 1: adding config "v" = "2"
Port 1: adding config "d" = "10"
Command line: ./ptp_video -i eth1 -CM_EXT -v2 -d10
Found Configuration for 1 ports
(1) Syn1588Ifc: Device /dev/syncD0 found
(1) syn1588(R) Hardware Clock M 2.3.2 f=125000000 Hz
(1) syn1588(R) PCIe NIC, Build 808 with HQ Oscillator
(1) Clk: Using Oregano Systems; syn1588(R) PCIe NIC; 8C:A5:A1:00:00:6B
(1)   with ClockId 8C:A5:A1:FF:FE:00:00:6B
(1) Activated SO_TIMSTAMPING hardware
(1) Activated SO_TIMSTAMPING hardware
(1) Clk: Resetting filters
(1) Init shared mem
(1) syn1588HwClk: UTC offset changed to 37 s
(1) State Change Initializing -> Listening
(1) State Change Listening -> Master
```

Step 3: Start vSync utility with digital mode

Open a syn1588 shell and start the syn1588 vsync utility by using the command "./vsync". Add the parameters "-d 0" (card number identified in step 1), choose the selected video mode using "-m 625i" (for this example the video mode ST170 PAL interlaced, 25Hz), "-t digital" to request digital sync signal output and optionally define a verbosity level for the output by "-v 2" (loglevel 2 includes errors and warnings). One can also redirect the log output to a file using the "-f filename" command line option.

Figure 10 Open syn1588 shell

```
root@ubuntu:/opt/oregano# ./vsync -m625i -t digital -v2
syn1588(R) vSync - Video Synchronization Engine
Build date: May 24 2017 - V 1.4-39 Rev g333a7dc
Copyright (c) Oregano Systems - Design & Consulting GesmbH 2005-2017
Confidential unpublished data - All rights reserved

Command line: ./vsync -m625i -t digital -v2
Syn1588Ifc: Device /dev/syncD0 found
syn1588(R) Hardware Clock M 2.3.2 f=125000000 Hz
syn1588(R) PCIe NIC, Build 808 with HQ Oscillator
Opening Shared Memory...
Init shared mem
Associated PTP instance: 001ec0ffff85ef8b_001
Video Processing started
SyncGen: Starting Genlock with rate 2 at 1167.056825960
SyncGen: Genlock settings
         frac_num:    0
         frac_denum:  0
         frame count: 625
         start time:  1167.680000000
         event ctrl:  0x00008158
         genlock ctrl:0x00000018
         frac_num:    0x01ffffff
         frac_denum:  0x00000000
HSYNC & FrameSYNC signals are digitally generated by the FPGA
and Period0 is routed on SMA X7 and FrameSYNC on SMA X6
```

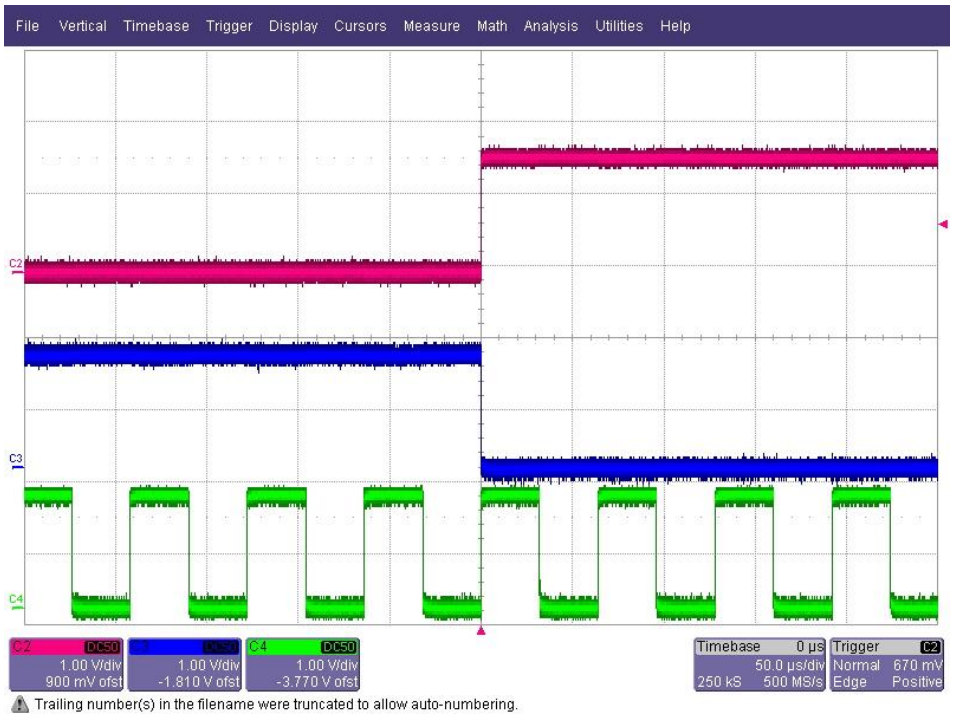

Figure 11 Digital Video Mode 625i (master operation)

Figure 11 shows the digital frame sync signal (channel 3 / blue) for the digital video Mode 625i, the 1 PPS signal from the syn1588® PCIe NIC (channel 2 / red) and the Period 0 signal (channel 4 / green). One may configure the GENLOCKCTRL register (as defined in an_register_map.pdf), to output HSYNC

signal instead of Period0 signal. The frame sync signal is perfectly phase locked to the 1 PPS master reference signal. One can use the oscilloscope or any video test equipment to verify this behavior.

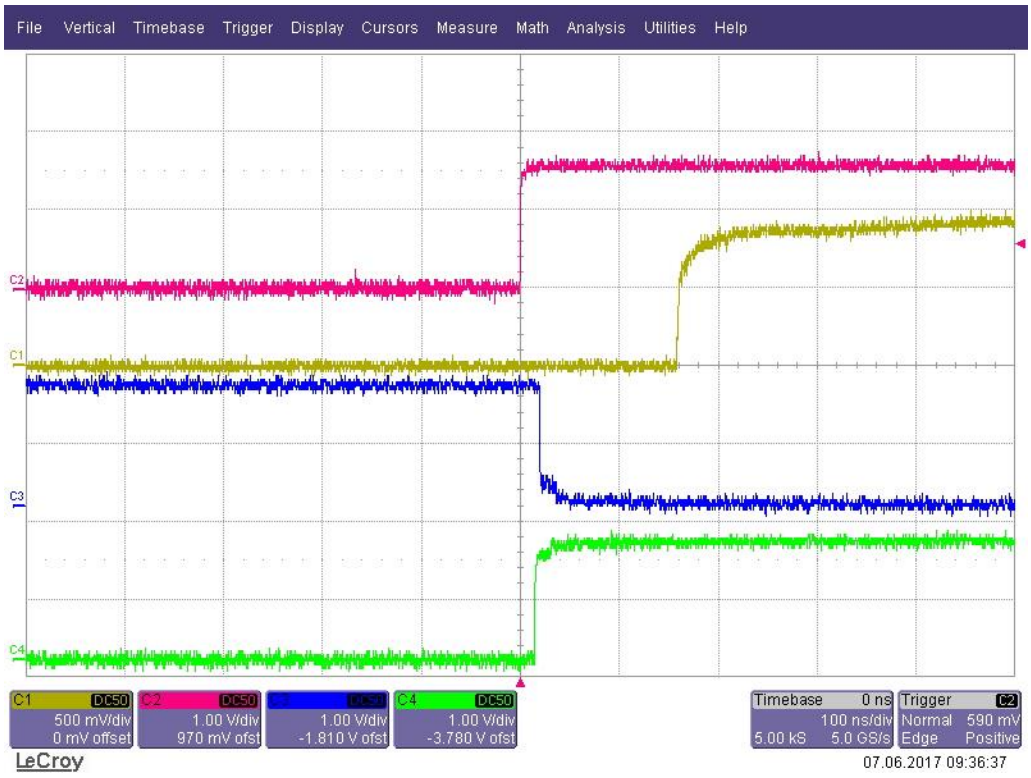

Figure 12 Digital Video Mode 625i (slave operation) – detail view

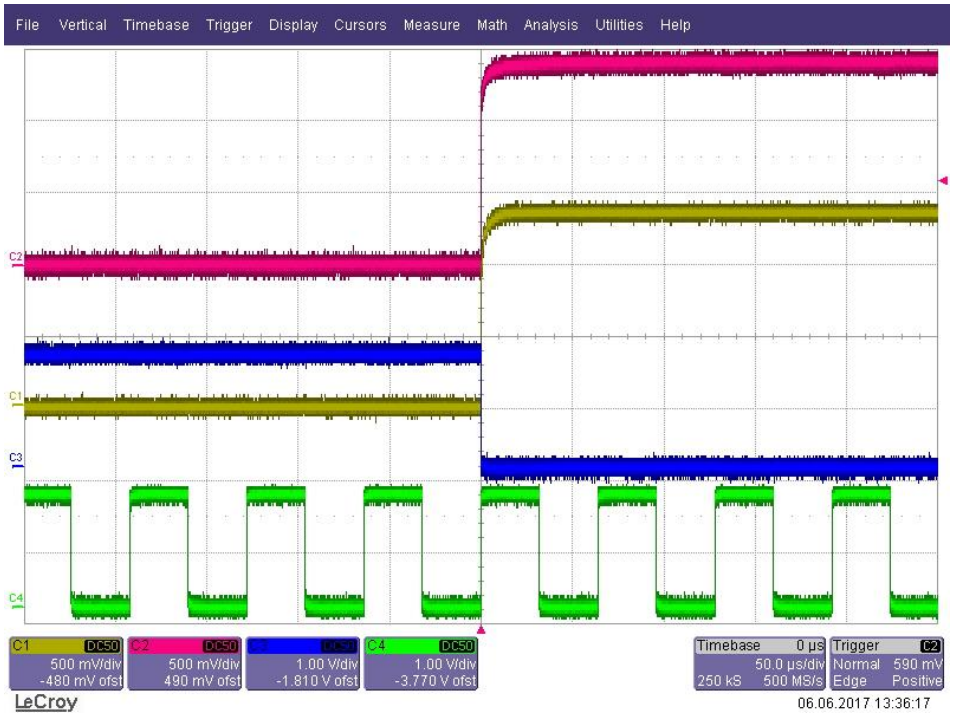

Figure 13 Mode 625i (slave operation) – overview

Figure 12 shows the 1PPS reference signal from the master (channel 1 / yellow), the local 1PPS signal (channel 2 / yellow), the digital frame sync signal (channel 3 / blue) for the digital video Mode 625i for the digital video Mode 625i and the PERIOD0 signal (channel 4 / green). One may configure the card to output HSYNC signal instead of PERIOD0 signal. Please contact Oregano Systems support if you require this mode.

The syn1588® PCIe NIC acts as slave and is synchronized to the master reference. The frame sync signal is phase locked to the 1 PPS of the Grandmaster in the network. The jitter between the 1 PPS of Grandmaster signal and the generated frame sync signal depends on the clock synchronization accuracy. The delay between the 1 PPS of master and slave is due to the cable delay from the 1 PPS output of the master and the oscilloscope. While Figure 12 shows a detailed view allowing to analyse the offset, Figure 13 shows the overview of the signals (the big picture).

Literature

AN002. (Version 2.8 - March 2019). *Application Note: "Ordering syn1588® PCIe NIC Revsion 2.1".* Oregano Systems.

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