

syn1588®

Version 1.4 – January 2020

Abstract

The syn1588® PCIe NIC allows the connection of an external GPS receiver that provides the absolute time for IEEE1588 master operations. This application note briefly describes the requirements for selecting an appropriate GPS receiver.

Requirements

Basically, almost every GPS receiver provides both a 1 PPS signal as well as a serial NMEA0183 stream (via UART). Both, the 1PPS signal and the serial NMEA data stream are required for PTP synchronization.

Please note that when connecting a GPS receiver to a syn1588® PCIe NIC one operate the syn1588® unit as IEEE1588 master. Please further note, that we generally recommend the high-stability OCXO option for all IEEE1588 master applications.

Meinberg GPS Solution

If one requires a reliable and accurate solution, Oregano Systems recommends GPS receivers from Meinberg (<http://www.meinberg.de>). For example the

Meinberg GPS180

(<http://www.meinbergglobal.com/english/products/3u-gps-clock-lc-display.htm>).



Figure 1 Meinberg GPS180

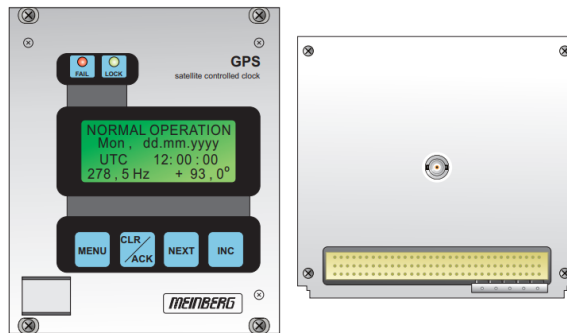


Figure 2 Meinberg GPS180 (front/rear view basic configuration)

Required Equipment for Meinberg GPS180

Connector: 96-pin VG-female DIN 41612 a+b+c

Ordering @ Meinberg: part number.: GPS180_V140_CON

Ordering @ Digikey: manufacturer: Harting, part number: 09032966845

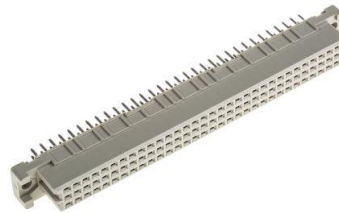


Figure 3 96-pin VG-female DIN 41612 a+b+c

Pin	Type
1	VCC in (+5V)
2	VCC in (+12V)
3	PPS out
4	GND
5	PPS in
6	GND
7	TC_DCLS in
8	TC_AM in
9	Reserve 0
10	GND
11	-4.096MHz in
12	+4.096MHz in
13	GND
14	Board_ID0
15	Board_ID1
16	Board_ID2
17	Board_ID3
18	Time Sync in
19	GND
20	10MHz in
21	GND
22	Reserve 1
23	RxD in
24	Slot_ID0
25	Slot_ID1
26	Slot_ID2
27	Slot_ID3
28	+USB
29	-USB
30	GND
31	GND
32	GND

Table 1 Pin assignment GPS180

Attenuator: 3db for 1PPS



Figure 4 Attenuator 3DB 50Ohm SMA

Ordering @ Digikey: Manufacturer: Crystek Corporation, part number: CATTEN-03R0

Cable: USB-A to open end



Figure 5 Cable USB-A to open end

Ordering @ Digikey: Manufacturer: Molex, part number: 0887283200

Test setup with Meinberg GPS180

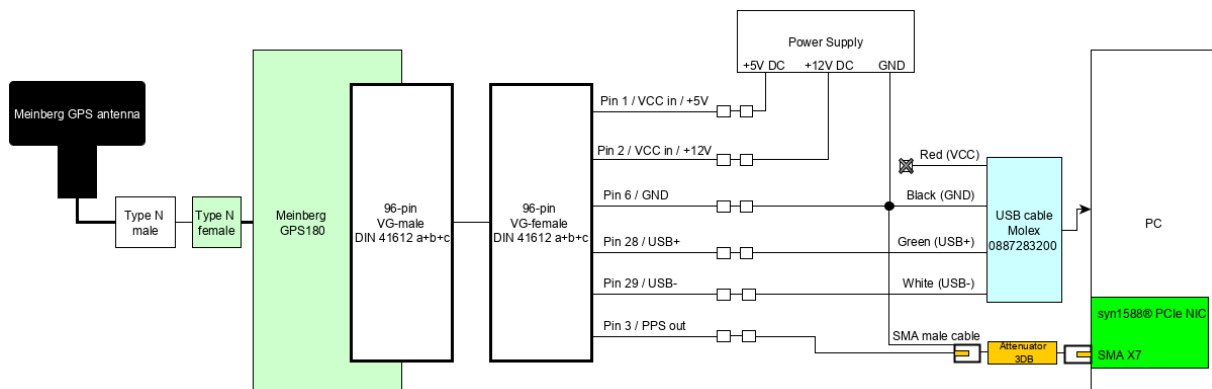


Figure 6 Meinberg Test setup

Navilock GPS Solution

If one requires a simple device for testing, a Navilock receiver (<https://www.navilock.com/>) is fine as well. For example the

Navilock NL-8004P

(https://www.navilock.com/produkte/G_62527/merkmale.html).



Figure 7 Navilock NL-8004P



Figure 8 Navilock Connector MD6 male

Required Equipment for Navilock NL-8004P

Cable: Navilock 62928



Figure 9 Navilock MD6 female serial > 5 x open wire LVTTTL (3.3 V) 52 cm cable

Ordering @ Navilock: part number: 62928

Cable: FTDI TTL-232R-3V3-WE



Figure 10 FTDI TTL-232R-3V3-WE cable

Ordering @ Digikey: Manufacturer: FTDI, part number: TTL-232R-3V3-WE

Cable: SMA male to open end



Figure 11 SMA male cable

Resistor: 10k Ohm



Figure 12 Resistor 1k2 Ohm

Test setup with Navilock NL-8004P

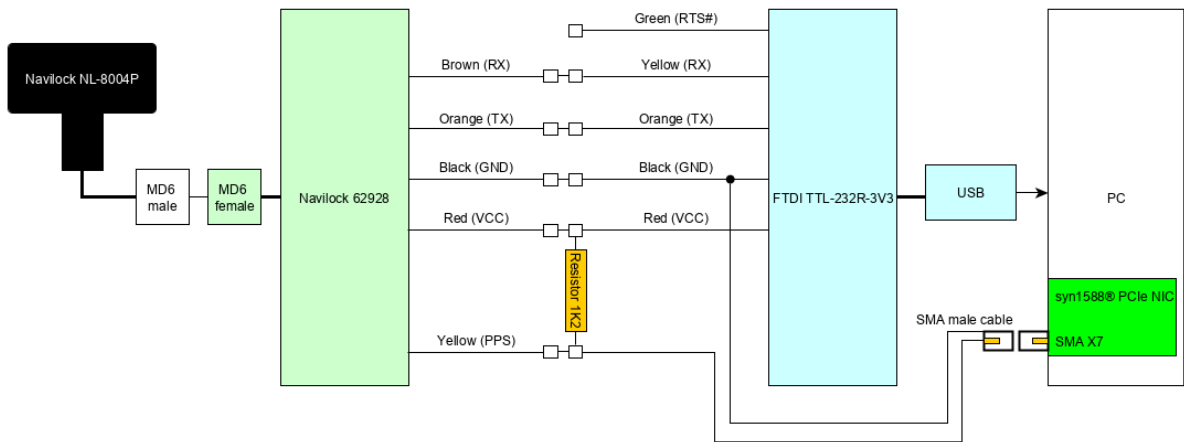


Figure 13 Navilock Test setup

Example eSync output

This example shows the eSync console output while synchronizing the syn1588® PCIe NIC to an Navilock NL-8004P GPS receiver by using an 1 PPS signal and the serial NMEA data stream. For detailed information on how to use eSync please refer to our syn1588® User Guide chapter 7.2 “eSync - Synchronizing to External Sources”

```
C:\Users\admin\Desktop\ptpmmmGUI_build_v1.8-17-
g0e6d01ad\sw\apps\windows>esync.exe -c COM7 -b 9600 -p1 -v2
syn1588(R) eSync - External Synchronization Engine
Build date: Aug  5 2019 - V 1.9-12 Rev gf5928642
Copyright (c) Oregano Systems - Design & Consulting GesmbH 2005-2018
Confidential unpublished data - All rights reserved


Please note that Oregano Systems' eSync utility is not SyncE -
Synchronous Ethernet

Command line: esync.exe -c COM7 -b 9600 -p1 -v2
Port 0: adding config "c" = "COM7"
Port 0: adding config "b" = "9600"
Port 0: adding config "p" = "1"
Port 0: adding config "v" = "2"
Syn1588Ifc requires at least:
- linux driver version 1.4-15-g05b7283
- windows driver version 10/05/2017, 10.9.16.182
syn1588(R) Hardware Clock M 2.3.3 f=125000000 Hz
syn1588(R) PCIe NIC Revision 2, Build 825 with HQ Oscillator
Clk: Using Oregano Systems; syn1588(R) PCIe NIC Revision 2;
00:1E:C0:85:D0:FD
    with ClockId 00:1E:C0:FF:FE:85:D0:FD
Clk: Resetting servos
Clk: Resetting filters
Using Nmea and PPS for synchronization
Warning: RMC message not detected.
Warning: No valid reference time received
Using external synchronization source with reference time
Starting synchronization process
Warning: RMC message not detected.
Warning: No valid reference time received
Update M2S-Delay -3 ns
Starting slew lock
Update M2S-Delay -1000000010 ns
Clk: Timestamp out of range: 1569855271.000000032
Update M2S-Delay -1000000008 ns
Clk: Timestamp out of range: 1569855272.000000032
Update M2S-Delay -999999982 ns
Clk: Setting time to Origin : 1569855273.000000032
Clk: Resetting servos
Clk: Resetting filters
Warning: RMC message not detected.
Warning: No valid reference time received
Update M2S-Delay -260464769 ns
Update M2S-Delay 739535319 ns
Clk: Timestamp out of range: 1569855274.000000032
Update M2S-Delay 739535383 ns
Clk: Timestamp out of range: 1569855275.000000032
Update M2S-Delay 739535471 ns
Clk: Setting time to Origin : 1569855276.000000032
Clk: Resetting servos
Clk: Resetting filters
Update M2S-Delay -5544280 ns
```



```
Update M2S-Delay -5544200 ns
Update M2S-Delay -5544112 ns
Update M2S-Delay -5544040 ns
Update M2S-Delay -5543960 ns
Update M2S-Delay -5543888 ns
Update M2S-Delay -5543800 ns
Update M2S-Delay -5543736 ns
Update M2S-Delay -5543648 ns
DriftCalc: drift is 81 ns/s
Clk: Resetting filters
Drift calc completed
Update M2S-Delay -5543665 ns
Update M2S-Delay -5543658 ns
Update M2S-Delay -5543651 ns
Update M2S-Delay -18728 ns
Clk: Resetting filters
Clk: slewed clock.
changing state to EFastFiltering
Update M2S-Delay 100 ns
Update M2S-Delay 83 ns
Update M2S-Delay 90 ns
Adjusting clock at 90.00 ns offset
Update M2S-Delay 49 ns
Adjusting clock at 19.00 ns offset
Update M2S-Delay -7 ns
Adjusting clock at -7.00 ns offset
Update M2S-Delay -1 ns
Adjusting clock at -1.00 ns offset
Update M2S-Delay -6 ns
Adjusting clock at -6.00 ns offset
Clk: Sync in bound      : 1569855300.005156207 Ofs:      -6 ns
Update M2S-Delay -12 ns
Adjusting clock at -12.00 ns offset
Update M2S-Delay -7 ns
```

Example eSync output

 <p>Oregano Systems A Meinberg Company</p> <p>Franzosengraben 8 A-1030 Vienna Austria http://oregano.at contact@oregano.at</p>	<p>Copyright © 2020 Oregano Systems – Design & Consulting GmbH ALL RIGHTS RESERVED.</p> <p>Oregano Systems does not assume any liability arising out of the application or use of any product described or shown herein nor does it convey any license under its patents, copyrights, or any rights of others.</p> <p>Licenses or any other rights such as, but not limited to, patents, utility models, trademarks or tradenames, are neither granted nor conveyed by this document, nor does this document constitute any obligation of the disclosing party to grant or convey such rights to the receiving party.</p> <p>Oregano Systems reserves the right to make changes, at any time without notice, in order to improve reliability, function or design. Oregano Systems will not assume responsibility for the use of any circuitry described herein.</p> <p>All trademarks used in this document are the property of their respective owners.</p>
--	--