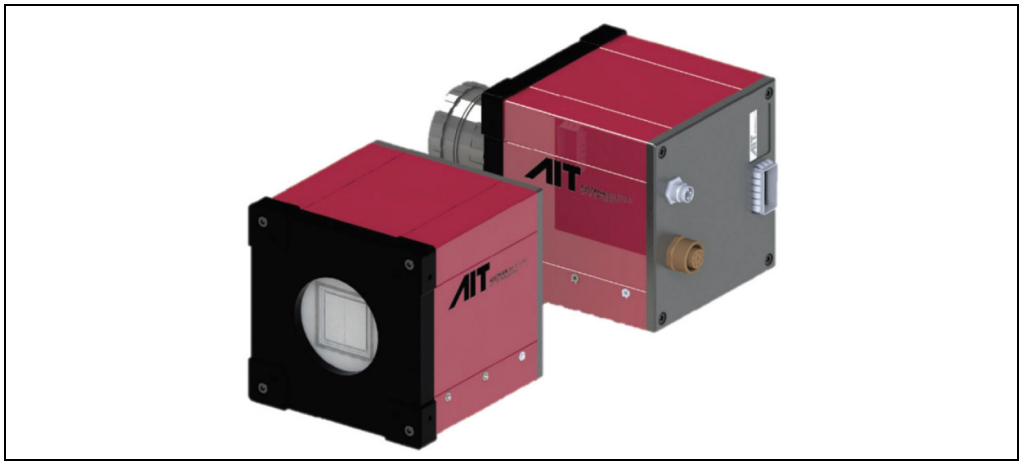
Version 1.1 – November 2016

Abstract

Designing a high-speed camera with integrated image processing requires dense packaging of both sensitive analog electronics as well as high speed digital processing power and communication. The solution: The PCBs are typically rigid-flex boards folded into the camera case.

Ultrafast Line-scan Camera



xposure camera

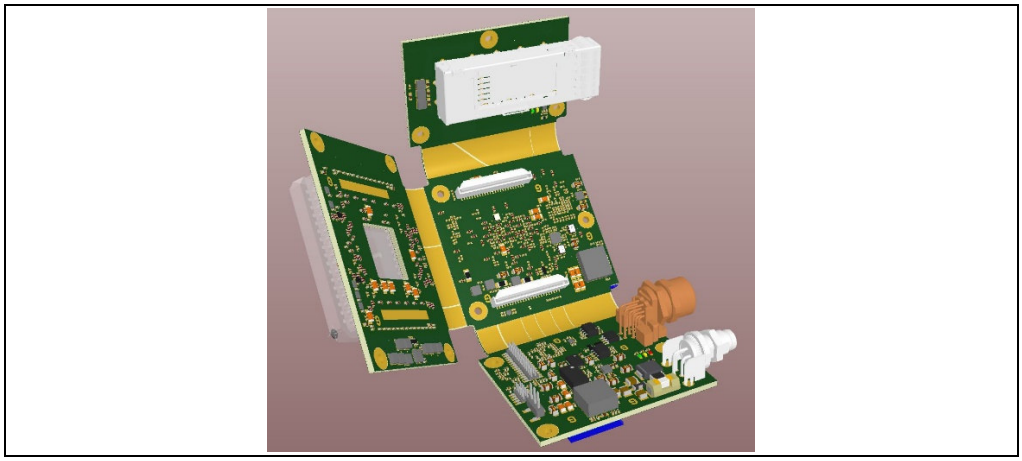
AIT's (Austrian Institute of Technology www.ait.ac.at/hpv) latest high-speed camera development, the **xposure camera,** offers impressive features

- 60x2016 pixels
- 600kHz line rate
- 40 Gbit Ethernet interface
- in-system hardware based image pre-processing
- small size 85 x 85 x 85 mm

PCB Design

Packing all these features into such a small volume created a huge challenge for the PCB design. A single rigid-flex PCB had been designed to meet the requirements of performance, power supply, high-speed interfaces, "quiet" analog circuitry and cooling. Four rigid areas are combined by flex areas allowing folding the PCB to a cube.

Early stage 3D-modelling was important to avoid interferences of components when folding the PCB. Additionally, the mechanics of both the camera and the cooling system had to be designed in parallel.



3D model

The electrical design was challenging as well. E.g. the placement of 900 components on this dense board. Both high-speed 10 Gbit/s lines as well as complex power supply structures had to be fed across the flex sections of the PCB. The length matching task for the DDR3 interface was demanding due to the dense packaging and small dimensions. We had to ensure that the sensitive analog circuitry like reference voltages and currents for the image sensor are not influenced by the high-speed digital processing and communication.

Technical Highlights

- 14 layer rigid-flex with symmetric stack up (4 layer polyimide flex, 10 layer rigid FR4)
- polyimide flex layer with no air gap between the layers
- overall board size: 171 mm x 121 mm
- Total components: 900
- Total holes: 3555, Min Hole size: laser drill 100µm, mechanical drill 200µm
- Blind vias (micro-via) between layer 1/2 and 13/14
- Buried vias: between layer 2/13
- Via in pad technology: Via plugging + plating over
- Impedance controlled: 90 Ω and 100 Ω differential pair; 45 Ω and 50 Ω single ended
- Back drilling of highspeed 10 Gbit vias
- 40 Gbit/s QSFP interface

More Challenges

Intel's latest high-end SoC FPGA Arria 10SX has been used allowing to implement a complex Linux based host system controlling the operation and communication of this high-speed line-scan camera. These SoC FPGA used on the PCB required a complex power distribution and power sequencing for both power-on as well as power-off.

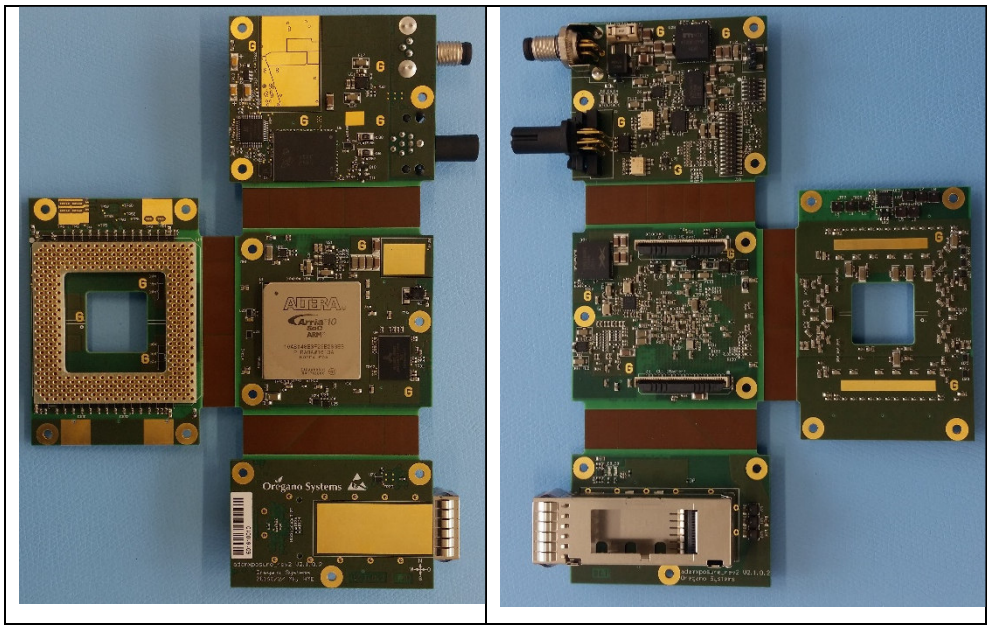
A challenge of designing leading edge technology: we even had to use engineering samples of the FPGAs. This means dealing with incomplete documentation, changing specifications of the FPGA and working around the usual silicon bugs. The power supply needed to provide three times the power just for the engineering samples.

Tools

Board level simulation has been used to verify the proper functions of all high-speed signals, the whole DDR3 interface, the clock distribution and selected, fast single ended signals. The overall engineering effort for the PCB design was approx. 24 person months. The design was done within 10 months. PCB design was done with Altium Designer while Mentor Graphics' HyperLynx has been used for the board level simulation.

Manufacturing of this PCB turned out to be complex, too. Only two PCB manufacturers were able to produce these PCBs at small volumes.

Results



xposure camera - PCB

All the effort was rewarded by a first-time right PCB design. All digital and analog electrical interfaces achieved their specified performance. AIT demonstrated the xposure line-scan camera at the VISION fair in Stuttgart/Germany this year.

AIT Austrian Institute of Technology

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As an Ingenious Partner to industry and public institutions, AIT is already researching and developing the technologies, methods and tools of tomorrow - paving the way for the innovations of the day after tomorrow.

More information: http://www.ait.ac.at/hpv

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