Version 1.16.0 - November 2022

Abstract

This application note describes how to use the video add-on function available for the syn1588® PCIe NIC Revision 2.1.

Introduction

The syn1588® PCIe NIC Revision 2.1 is optionally equipped with a video add-on board that allows generation of analog video sync signals. Ordering code is SYN1588PCI-Video. Lease see application note: “Ordering syn1588® PCIe NIC Revision 2.1” (AN002, Version 2.8 - March 2019) for details. This application note describes in detail how these video sync signals can be generated.

Note, there is no Video add-on option available for the Revision 2.3 of the syn1588® PCIe NIC.

Pre-Requisites

The following requirements have to be met in order to generate video sync signals using the syn1588® PCIe NIC with the video add-on option:

Figure 1 syn1588® PCIe NIC with the video add-on option

- syn1588® PCIe NIC with the Video Add-on option
- driver software for the syn1588® PCIe NIC
- syn1588® PTP Stack

- vSync utility
- Administrator rights to run the syn1588® software

All software may be found on the wooden syn1588® USB stick that comes with every syn1588® PCIe NIC.

Figure 2 syn1588® USB stick

Optionally, the software can be downloaded from the Oregano Systems secure file server. Please contact Oregano Systems support (support@oregano.at) in order to receive an account for this secure file server.

Note, the video add-on board is currently not available for the syn1588® Dual NIC. Thus, the utility vSync cannot be used in context with a syn1588® Dual NIC.

The vSync Utility

There is a dedicated utility vSync that controls the generation of the video sync signals. The following listing shows the usage screen of vSync:

```
2022-01-04 13:59:46.864592 [INFO    ] [             ]  syn1588(R) vSync - Video
Synchronization Engine
2022-01-04 13:59:46.869693 [INFO    ] [             ]  Build date: 2022-01-
04T10:06:51 - v1.14-0-g6624ce7d
2022-01-04 13:59:46.870184 [INFO    ] [             ]  Copyright (c) Oregano
Systems - Design & Consulting GesmbH 2005-2022
2022-01-04 13:59:46.871460 [INFO    ] [             ]  Confidential unpublished
data - All rights reserved
2022-01-04 13:59:46.871739 [INFO    ] [             ]  Command line: vsync -h
usage: vsync [-h][-d card][-I clockID][-f filelog][-m videoMode]
[-o ptpPort][-t dacTiming][-c offsetCompensate][-v logLevel]

  -h                  shows this usage screen
  -d card             select the device driver (syn1588 card number) [0]
  -I clockID          specify clock identity to use for syn1588 card
identification
                        e.g.: "00:04:A3:FF:FE:4B:1B:67",
                        this will be used instead of "-d|card"
  -D useClockID       if this is [true] the provided clockID will be used
                        to select the correct syn1588 card, default: [false]
  -B boundaryClock    set this to [true] if you want to interact with a PTP
                        Stack operating as PTP boundary Clock, default: [false]
  -O bcPortAmount     set the amount of ports handled by the PTP boundary clock
                        only applicable if the boundarClock mode is enabled,
default: [1]
  -o ptpPort          set the PTP port number for the connected PTP Stack [1]
                        if the boundarClock mode is enabled this defines the first
port
                          all other ports (bcPortAmount) are incrementally
numbered
                          e.g., 1, 2, 3, 4 for bcPortAmount = 4 and ptpPort = 1
                          e.g., 3, 4 for bcPortAmount = 2 and ptpPort = 3
  -f filelog            write log output to the given file
                        (e.g., "/home/user/status.log" or "C:\work\status.log")
                        instead of output to stdout
  -m videoMode        select the desired video mode. disabled by default[0]
                      525i     ST170 NTSC interlaced (525i 30/1001 Hz)
                      625i     ST170 PAL  interlaced (625i 25 Hz)
                      720p50   ST296, 3, progressive     (720p 50 Hz)
                      720p59   ST296, 2, progressive     (720p 60/1001 Hz)
                      1080i50  ST274, 6, interlaced      (1080i 50 Hz)
                      1080i59  ST274, 5, interlaced      (1080i 60/1001 Hz)
                      1080p50  ST274, 3, progressive     (1080p 50 Hz)
                               not supported by DAC, digital only
                      1080p59  ST274, 2, progressive     (1080p 60/1001 Hz)
                               not supported by DAC, digital only
  -t dacTiming        select if DAC is used or only digital sync signals used
[DAC]
                      DAC     - output Timing for the Video DAC Add-on board
                      digital - output Timing for digital sync signals
  -c offsetCompensate set offset to adjust in +/- [nano seconds]      [0]
                        selectable range (-32768 ns to 32767 ns)
  -H enableHSync      output of Hsync instead of Period0 to SMA-ports in
                        digital mode.
  -A enableAudioSignals enable generation of Audio signals,
                          if syn1588 hardware supports it
  -E enableExtendedVideoSignals enable generation of additional SDI Video signals,
                                  if syn1588 hardware supports it
  -L SDI_LTC_dateFormat enable generation of SDI LTC Timecode,
                          either in "DDMMYY" or "MJD" format,
                          if syn1588 hardware supports it
  -v loglevel     change verbosity level
                    (off, critical, error, warning, info, debug, trace) [info]
```

Quick Start: Generating an Analog Video Sync Signal

Step 1; Identify your syn1588® PCIe NIC

Open a syn1588® shell and start the syn1588® utility by using the command "./syn1588". In our example we just have one syn1588® PCIe NIC. If you have more than one syn1588® PCIe NICs in your system type the command "listcards" to identify your syn1588® PCIe NIC with mounted video adapter board.

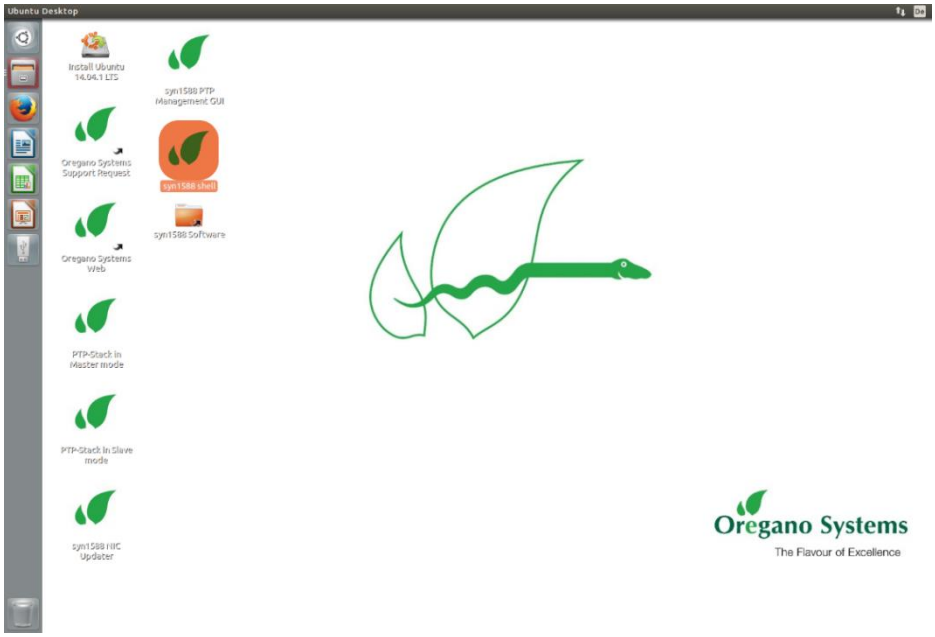

Figure 3 Open syn1588 shell

```
oregano@KAEFER:/opt/oregano/bin$ sudo ./syn1588
[sudo] password for oregano:
2022-01-07 12:28:30.408114 [INFO    ] [             ]  syn1588(R) Driver Interface
2022-01-07 12:28:30.408218 [INFO    ] [             ]  Build date: 2022-01-
05T12:43:16 - v1.14-9-g7cbf9e73
2022-01-07 12:28:30.408242 [INFO    ] [             ]  Copyright (c) Oregano
Systems - Design & Consulting GesmbH 2005-2022
2022-01-07 12:28:30.408268 [INFO    ] [             ]  Confidential unpublished
data - All rights reserved
2022-01-07 12:28:30.408357 [INFO    ] [syn1588      ]  Syn1588Ifc requires at
least:
2022-01-07 12:28:30.408384 [INFO    ] [syn1588      ]  - linux driver version 1.4-
15-g05b7283
2022-01-07 12:28:30.408404 [INFO    ] [syn1588      ]  - windows driver version
10/05/2017, 10.9.16.182
2022-01-07 12:28:30.408451 [INFO    ] [syn1588      ]  Device /dev/syncD0 found
2022-01-07 12:28:30.408503 [INFO    ] [syn1588      ]  syn1588(R) Hardware Clock M
2.3.5 f=125000000 Hz
2022-01-07 12:28:30.408535 [INFO    ] [syn1588      ]  Found stop clock support
2022-01-07 12:28:30.408572 [INFO    ] [syn1588      ]  Using MAC TS Version 3160
2022-01-07 12:28:30.408595 [INFO    ] [syn1588      ]  Using programmable 1-step
TS
Selected syn1588(R) card 0
```

After identifying your card number quit the syn1588 utility by using the “quit” command. Use command “ifconfig” to find out the Ethernet interface of your syn1588® PCIe NIC by comparing the MAC addresses. In our example it is “eth1”.

Caution:

Do not invoke the syn1588 utility after starting the vSync utility as the former initializes the Jitter Cleaner PLL which causes the PLL to loose lock. One may start the syn1588 utility in a separate shell and keep it open for purposes like re-configuring the IOMATRIX register, etc.

```
root@ubuntu:/opt/oregano# ifconfig
eth0      Link encap:Ethernet  HWaddr d0:50:99:2a:ef:05
          inet addr:192.168.102.192  Bcast:192.168.103.255
          inet6 addr: fe80::d250:99ff:fe2a:ef05/64 Scope:Link
          UP BROADCAST RUNNING MULTICAST  MTU:1500  Metric:1
          RX packets:18962 errors:0 dropped:0 overruns:0 frame:0
          TX packets:115 errors:0 dropped:0 overruns:0 carrier:0
          collisions:0 txqueuelen:1000
          RX bytes:3203506 (3.2 MB)  TX bytes:16051 (16.0 KB)

eth1      Link encap:Ethernet  HWaddr 8c:a5:a1:00:00:6b
          inet6 addr: fe80::8ea5:a1ff:fe00:6b/64 Scope:Link
          UP BROADCAST RUNNING MULTICAST  MTU:1500  Metric:1
          RX packets:5235 errors:0 dropped:0 overruns:0 frame:0
          TX packets:875 errors:0 dropped:0 overruns:0 carrier:63
          collisions:0 txqueuelen:1000
          RX bytes:471150 (471.1 KB)  TX bytes:13371102 (13.3 MB)
          Interrupt:16 Memory:90700000-90710000

lo        Link encap:Local Loopback
          inet addr:127.0.0.1  Mask:255.0.0.0
          inet6 addr: ::1/128 Scope:Host
          UP LOOPBACK RUNNING  MTU:65536  Metric:1
          RX packets:163 errors:0 dropped:0 overruns:0 frame:0
          TX packets:163 errors:0 dropped:0 overruns:0 carrier:0
          collisions:0 txqueuelen:0
          RX bytes:11774 (11.7 KB)  TX bytes:11774 (11.7 KB)
```

Step 2: Start syn1588® PTP Stack

Open a syn1588® shell and start the syn1588® PTP Stack by using the command "./ptp". Add the parameters "-i eth1" (interface identified in Step 1), "-C M_EXT" (Master on external reference), "-d 0" (Domain 0..255, default Domain is 0) and optional "-v info" (this loglevel includes errors, warnings and informational/status messages).

Alternatively if you want to run the syn1588® PTP Stack in other configuration for example as slave please choose one of your appreciated parameter:

-C options set Clock Class (0..255)

M_EXT....Master on external reference

M_HOLD...Master on external reference (in holdover)

M_NSYNC..Master on external reference (not sync'd)

M_SLAVE..Master on external reference (may be Slave)

S...Slave only

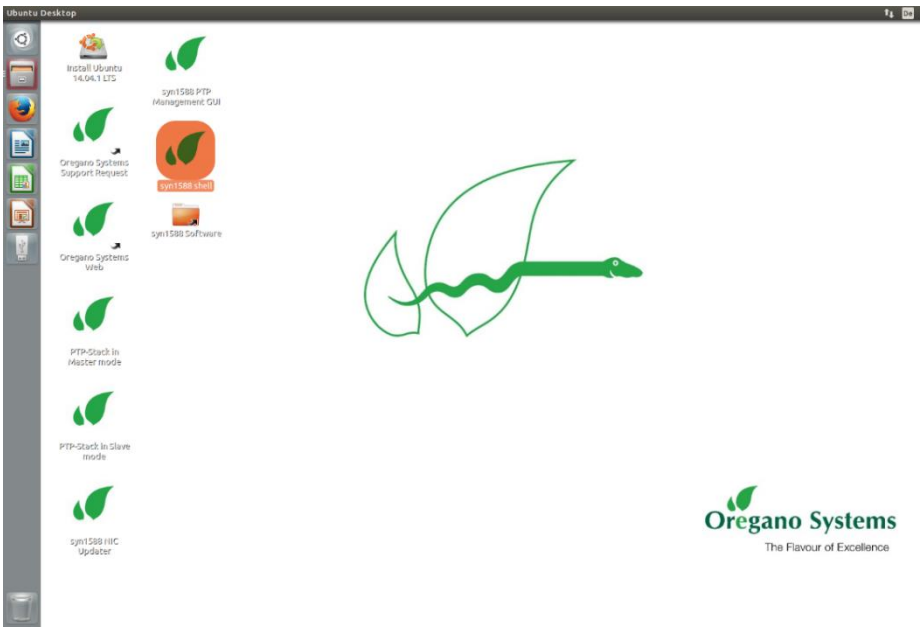

Figure 4 Open syn1588 shell

```
oregano@KAEFER:/opt/oregano/bin$ sudo ./ptp -i enp2s0 -C M_EXT -d 20 -v info
2022-01-07 12:31:12.562888 [INFO    ] [             ]  syn1588(R) PTP Stack -
IEEE1588-2008 Engine
2022-01-07 12:31:12.562922 [INFO    ] [             ]  Build date: 2022-01-
05T12:43:16 - v1.14-9-g7cbf9e73
2022-01-07 12:31:12.562927 [INFO    ] [             ]  Copyright (c) Oregano
Systems - Design & Consulting GesmbH 2005-2022
2022-01-07 12:31:12.562932 [INFO    ] [             ]  Confidential unpublished
data - All rights reserved
2022-01-07 12:31:12.562939 [INFO    ] [             ]  syn1588(R) PTP Stack
started: 2022-01-07 11:31:12.562937 (UTC)
2022-01-07 12:31:12.563036 [INFO    ] [p1           ]  Port 1: adding config "i" =
"enp2s0"
2022-01-07 12:31:12.563046 [INFO    ] [p1           ]  Port 1: adding config "C" =
"M_EXT"
2022-01-07 12:31:12.563051 [INFO    ] [p1           ]  Port 1: adding config "d" =
"20"
2022-01-07 12:31:12.563057 [INFO    ] [p1           ]  Port 1: adding config "v" =
"info"
2022-01-07 12:31:12.563063 [INFO    ] [p1           ]  PTP version 2.0
2022-01-07 12:31:12.563068 [INFO    ] [             ]  Command line: ./ptp -i
enp2s0 -C M_EXT -d 20 -v info
2022-01-07 12:31:12.563083 [WARNING ] [             ]  Failed to set high priority
for the PTP thread!
2022-01-07 12:31:12.563094 [INFO    ] [p1           ]  Found Configuration for 1
ports
2022-01-07 12:31:12.563328 [INFO    ] [syn1588      ]  Syn1588Ifc requires at
least:
2022-01-07 12:31:12.563337 [INFO    ] [syn1588      ]  - linux driver version 1.4-
15-g05b7283
2022-01-07 12:31:12.563342 [INFO    ] [syn1588      ]  - windows driver version
10/05/2017, 10.9.16.182
2022-01-07 12:31:12.563356 [INFO    ] [syn1588      ]  Device /dev/syncD0 found
2022-01-07 12:31:12.563373 [INFO    ] [syn1588      ]  syn1588(R) Hardware Clock M
2.3.5 f=125000000 Hz
2022-01-07 12:31:12.563382 [INFO    ] [syn1588      ]  Found stop clock support
2022-01-07 12:31:12.563394 [INFO    ] [syn1588      ]  Using MAC TS Version 3160
2022-01-07 12:31:12.563399 [INFO    ] [syn1588      ]  Using programmable 1-step
TS
2022-01-07 12:31:12.563431 [INFO    ] [syn1588      ]  syn1588(R) PCIe NIC
Revision 2, Build 865
2022-01-07 12:31:12.563448 [INFO    ] [p1           ]  Using syn1588 mode
2022-01-07 12:31:12.563477 [INFO    ] [p1.clock     ]  Spike M2S: Init with ival
0, buffer size 16
2022-01-07 12:31:12.563554 [INFO    ] [p1.clock     ]  Spike Path: Init with ival
0, buffer size 16
2022-01-07 12:31:12.563570 [INFO    ] [p1.io        ]  Init shared mem
2022-01-07 12:31:12.565766 [INFO    ] [syn1588      ]  syn1588HwClk: clearing leap
second jump
2022-01-07 12:31:12.565777 [INFO    ] [p1.engine    ]  Settings: ClockId
00:1e:c0:ff:fe:85:de:2b
2022-01-07 12:31:12.565784 [INFO    ] [p1.engine    ]  Settings: Prio1 128
ClkClass 6 clkAccuracy 39 clkVariance 65535
2022-01-07 12:31:12.565791 [INFO    ] [p1.engine    ]  Settings: Prio2 128 Domain
20
2022-01-07 12:31:12.565919 [INFO    ] [p1.network.mcport]  SIOCSHWTSTAMP: tx_type
1 requested, got 1; rx_filter 0 requested, got 12
2022-01-07 12:31:12.565930 [INFO    ] [p1.network.mcport]  Activated
SO_TIMESTAMPING hardware
2022-01-07 12:31:12.566027 [INFO    ] [p1.network.mcport]  SIOCSHWTSTAMP: tx_type
1 requested, got 1; rx_filter 0 requested, got 12
2022-01-07 12:31:12.566036 [INFO    ] [p1.network.mcport]  Activated
SO_TIMESTAMPING hardware
2022-01-07 12:31:12.566299 [INFO    ] [p1.clock     ]  Clk: Using Oregano Systems;
syn1588(R) PCIe NIC Revision 2; 00:1E:C0:85:DE:2B
2022-01-07 12:31:12.566308 [INFO    ] [p1.clock     ]    with ClockId
00:1e:c0:ff:fe:85:de:2b
2022-01-07 12:31:12.566445 [INFO    ] [p1.clock     ]  Clk: Resetting servos
```

```
2022-01-07 12:31:12.566450 [INFO    ] [p1.clock     ]  Clk: Resetting filters
2022-01-07 12:31:12.566456 [INFO    ] [p1.clock     ]  Spike M2S: Init with ival
0, buffer size 16
2022-01-07 12:31:12.566462 [INFO    ] [p1.clock     ]  Spike Path: Init with ival
0, buffer size 16
2022-01-07 12:31:12.566472 [INFO    ] [p1.io        ]  Init shared mem
2022-01-07 12:31:12.566485 [INFO    ] [syn1588      ]  syn1588HwClk: clearing leap
second jump
2022-01-07 12:31:12.566510 [INFO    ] [p1.engine    ]  1641555109.567559456s State
Listening
2022-01-07 12:31:13.566518 [INFO    ] [p1.engine    ]  State Change Initializing -
> Listening
2022-01-07 12:31:13.566614 [INFO    ] [syn1588      ]  syn1588HwClk: UTC offset
changed to 37 s
2022-01-07 12:31:13.566686 [INFO    ] [p1.engine    ]  1641555110.567732391s State
Listening
2022-01-07 12:31:14.566828 [INFO    ] [p1.engine    ]  1641555111.567874086s State
Listening
2022-01-07 12:31:15.567119 [INFO    ] [p1.engine    ]  1641555112.568164630s State
Listening
2022-01-07 12:31:16.567924 [INFO    ] [p1.engine    ]  1641555113.568970336s State
Listening
2022-01-07 12:31:17.568208 [INFO    ] [p1.engine    ]  1641555114.569253496s State
Listening
2022-01-07 12:31:18.568494 [INFO    ] [p1.engine    ]  1641555115.569540160s State
Listening
2022-01-07 12:31:19.568778 [INFO    ] [p1.engine    ]  1641555116.569823408s State
Listening
2022-01-07 12:31:19.745195 [INFO    ] [p1.engine    ]  State Change Listening ->
Master
2022-01-07 12:31:19.745271 [INFO    ] [p1.engine    ]  <--- Announce seqId: 1
2022-01-07 12:31:19.745470 [INFO    ] [p1.engine    ]  <--- Sync seqId: 1
2022-01-07 12:31:19.745684 [INFO    ] [p1.engine    ]  <--- FollowUp seqId: 1
2022-01-07 12:31:20.569310 [INFO    ] [p1.engine    ]  1641555117.570355113s State
Master
2022-01-07 12:31:20.569438 [INFO    ] [p1.engine    ]  <--- Announce seqId: 2
2022-01-07 12:31:20.745732 [INFO    ] [p1.engine    ]  <--- Sync seqId: 2
2022-01-07 12:31:20.745878 [INFO    ] [p1.engine    ]  <--- FollowUp seqId: 2
2022-01-07 12:31:21.569849 [INFO    ] [p1.engine    ]  1641555118.570879690s State
Master
2022-01-07 12:31:21.746256 [INFO    ] [p1.engine    ]  <--- Sync seqId: 3
2022-01-07 12:31:21.746432 [INFO    ] [p1.engine    ]  <--- FollowUp seqId: 3
2022-01-07 12:31:22.570358 [INFO    ] [p1.engine    ]  1641555119.571403875s State
Master
```

Step 3: Start vSync utility with analog mode

Open a syn1588® shell and start the syn1588® vSync utility by using the command "./vsync". Add the command line parameters "-d 0" (card number identified in step 1), choose the selected video mode using "-m 625i" (for this example the video mode ST170 PAL interlaced, 625i, 25Hz is used) and optionally define a verbosity level for the output by "-v info" (this loglevel includes errors, warnings and info/status output). One can also redirect the log output to a file using the "-f filename" command line option.

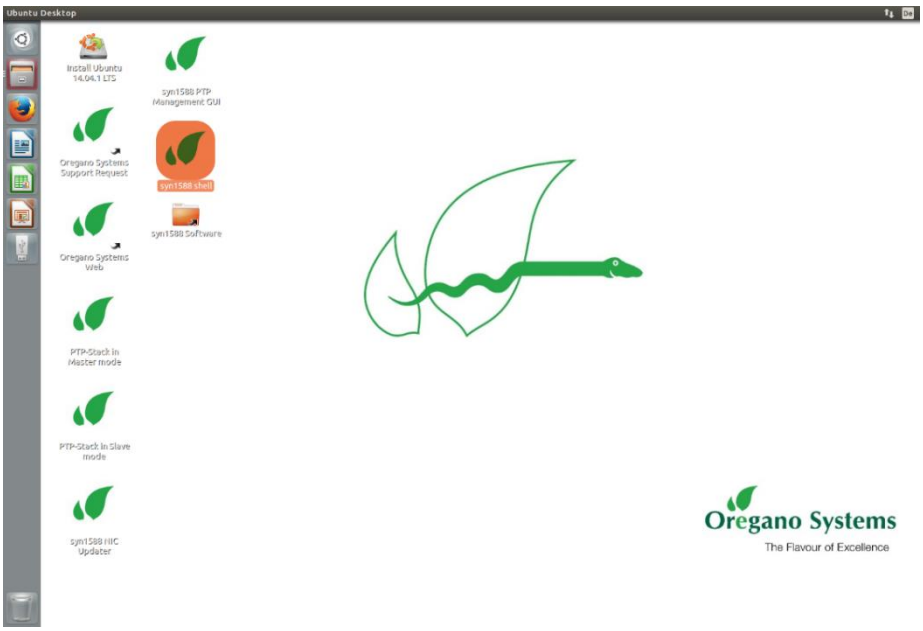

Figure 5 Open syn1588 shell

```
oregano@KAEFER:/opt/oregano/bin$ sudo ./vSync -d 0 -m 625i -v info
2022-01-07 12:38:38.441471 [INFO    ] [             ]  syn1588(R) vSync - Video
Synchronization Engine
2022-01-07 12:38:38.441502 [INFO    ] [             ]  Build date: 2022-01-
05T12:43:16 - v1.14-9-g7cbf9e73
2022-01-07 12:38:38.441508 [INFO    ] [             ]  Copyright (c) Oregano
Systems - Design & Consulting GesmbH 2005-2022
2022-01-07 12:38:38.441513 [INFO    ] [             ]  Confidential unpublished
data - All rights reserved
2022-01-07 12:38:38.441517 [INFO    ] [             ]  Command line: ./vSync -d 0
-m 625i -v info
2022-01-07 12:38:38.441541 [INFO    ] [             ]  Port 0: adding config "d" =
"0"
2022-01-07 12:38:38.441550 [INFO    ] [             ]  Port 0: adding config "m" =
"625i"
2022-01-07 12:38:38.441556 [INFO    ] [             ]  Port 0: adding config "v" =
"info"
2022-01-07 12:38:38.441562 [INFO    ] [syn1588      ]  Syn1588Ifc requires at
least:
2022-01-07 12:38:38.441571 [INFO    ] [syn1588      ]  - linux driver version 1.4-
15-g05b7283
2022-01-07 12:38:38.441576 [INFO    ] [syn1588      ]  - windows driver version
10/05/2017, 10.9.16.182
2022-01-07 12:38:38.441592 [INFO    ] [syn1588      ]  Device /dev/syncD0 found
2022-01-07 12:38:38.441619 [INFO    ] [syn1588      ]  syn1588(R) Hardware Clock M
2.3.5 f=125000000 Hz
2022-01-07 12:38:38.441638 [INFO    ] [syn1588      ]  Found stop clock support
2022-01-07 12:38:38.441649 [INFO    ] [syn1588      ]  Using MAC TS Version 3160
2022-01-07 12:38:38.441654 [INFO    ] [syn1588      ]  Using programmable 1-step
TS
2022-01-07 12:38:38.441673 [INFO    ] [syn1588      ]  syn1588(R) PCIe NIC
Revision 2, Build 865
2022-01-07 12:38:38.441710 [INFO    ] [1.sharedmemory.api.io]  Init shared mem
2022-01-07 12:38:39.502762 [ERROR   ] [Main         ]  No PTP port is qualified
for operation, stopping video signal generator!
2022-01-07 12:38:40.502979 [ERROR   ] [Main         ]  No PTP port is qualified
for operation, stopping video signal generator!
2022-01-07 12:38:41.503184 [ERROR   ] [Main         ]  No PTP port is qualified
for operation, stopping video signal generator!
2022-01-07 12:38:42.502397 [ERROR   ] [Main         ]  No PTP port is qualified
for operation, stopping video signal generator!
```

```
2022-01-07 12:38:43.502610 [ERROR   ] [Main         ]  No PTP port is qualified
for operation, stopping video signal generator!
2022-01-07 12:38:45.502987 [INFO    ] [Main         ]  Video Processing started
2022-01-07 12:38:45.503036 [INFO    ] [Main.VideoDAC]  Trying to enable pll with
frequency: 27000000
2022-01-07 12:38:45.866805 [INFO    ] [Main.VideoDAC]  PLL was configured
successfully!
2022-01-07 12:39:07.150144 [INFO    ] [Main.VideoDAC]  PLL is locked
2022-01-07 12:39:07.204413 [INFO    ] [Main.SDIAudio]  Starting SDI counter at the
next full second 1641555585
2022-01-07 12:39:07.204466 [INFO    ] [Main.SDIAudio]  SDI 27 MHz counter:
4179549376
2022-01-07 12:39:07.204492 [INFO    ] [Main.SDIAudio]  SDI 90 kHz counter:
1717602192
2022-01-07 12:39:07.204596 [INFO    ] [Main.SDIAudio]  Starting Video Signal
generation for video mode 625i
2022-01-07 12:39:07.204986 [INFO    ] [Main         ]  starting generation of
video signals at time: 1641555584.201975347
2022-01-07 12:39:07.209516 [INFO    ] [Main.VideoDAC]  DAC output is enabled
```

Figure 6 Analog Video Mode 625i (master operation)

Figure 6 shows the video output (channel 1 / yellow) for the analog video Mode ST170 PAL interlaced, 625i 25Hz and the 1 PPS signal from the syn1588® PCIe NIC (channel 2 / red). The video signal is now perfectly phase locked to the 1 PPS master reference signal. One can use the oscilloscope or any video test equipment to verify this behavior.

Note:

For better understanding of the video output signal, the figure above has been generated with a test-version of the syn1588® PCIe NIC, where not all video-data-bits have been set to zero. In the production version, the data-bits are all set to zero, which generates the so-called “Genlock” signal. But then there

would be no visible difference between video signal and blank signal in the figure, except the doubled HSYNC pulse frequency during V-blank.

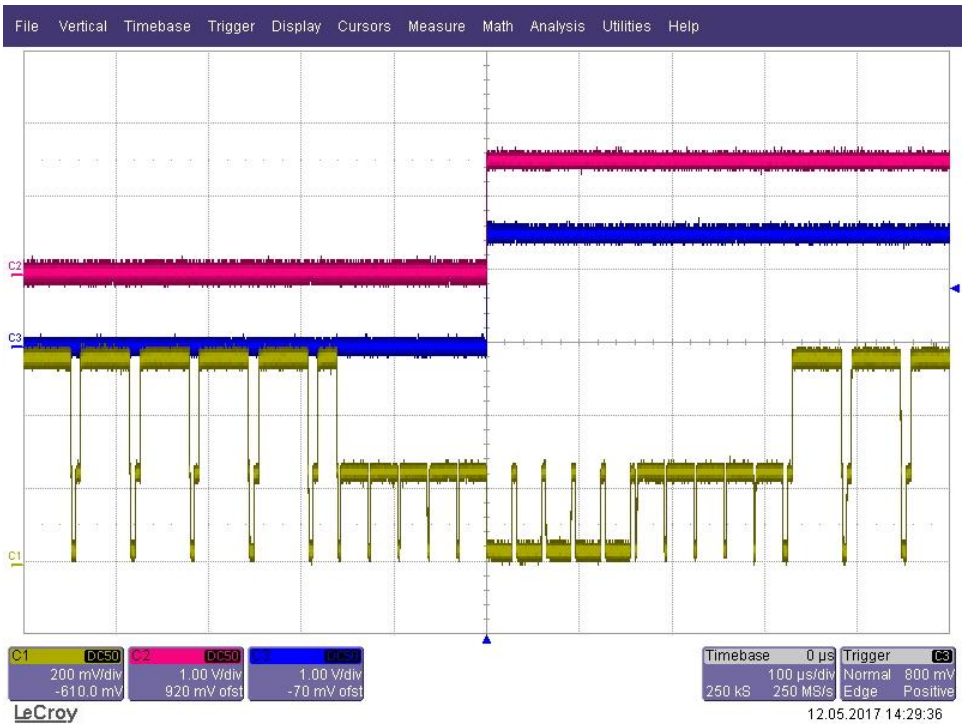

Figure 7 Analog Video Mode 625i (slave operation)

Figure 7 shows the video output (channel 1 / yellow) for the analog video Mode 625i (ST170 PAL interlaced, 25Hz), the 1 PPS signal from the syn1588® PCIe NIC (channel 2 / red) and the 1 PPS signal from the master reference clock (channel 3 / blue). The syn1588® PCIe NIC now acts as slave and is synchronized to an external reference master. The video signal is phase locked to the 1 PPS of the Grandmaster in the network. The jitter between the 1PPS Grandmaster signal and the generated video sync signal depends on the clock synchronization accuracy.

Note:

For better understanding of the video output signal, the figure above has been generated with a test-version of the syn1588® PCIe NIC, where not all video-data-bits have been set to zero. In the production version, the data-bits are all set to zero, which generates the so-called “Genlock” signal. But then there would be no visible difference between video signal and blank signal in the figure, except the doubled HSYNC pulse frequency during V-blank.

Quick Start: Generating a Digital Video Sync Signals

Step 1: Identify your syn1588® PCIe NIC

Open a syn1588 shell and start the syn1588 utility by using the command "./syn1588". In our example we just have one syn1588® PCIe NIC. If you have more than one syn1588® PCIe NICs in your system type the command "listcards" to identify your syn1588® PCIe NIC with mounted Video adapter board.

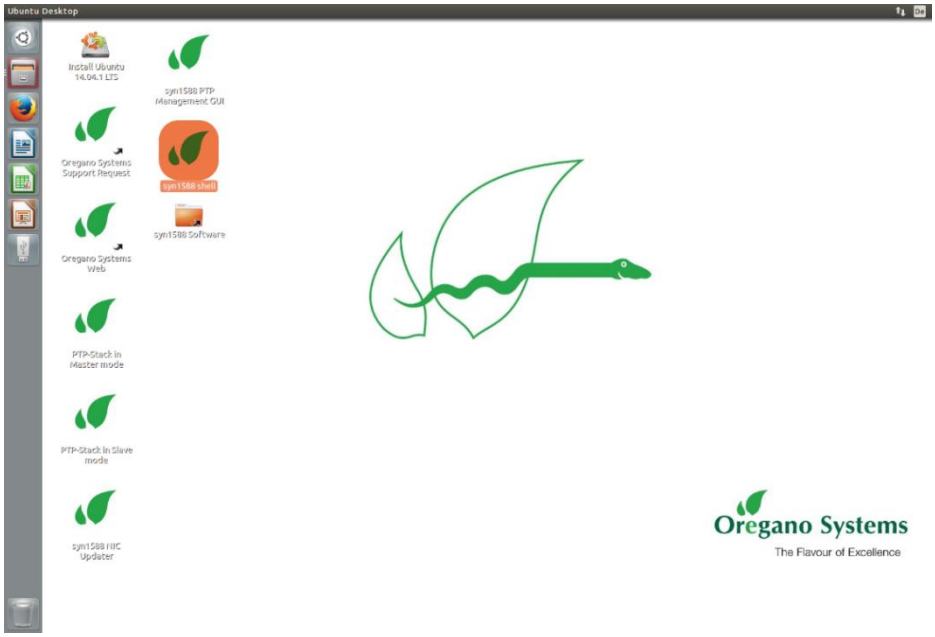

Figure 8 Open syn1588 shell

```
oregano@KAEFER:/opt/oregano/bin$ sudo ./syn1588
[sudo] password for oregano:
2022-01-07 12:28:30.408114 [INFO    ] [             ]  syn1588(R) Driver Interface
2022-01-07 12:28:30.408218 [INFO    ] [             ]  Build date: 2022-01-
05T12:43:16 - v1.14-9-g7cbf9e73
2022-01-07 12:28:30.408242 [INFO    ] [             ]  Copyright (c) Oregano
Systems - Design & Consulting GesmbH 2005-2022
2022-01-07 12:28:30.408268 [INFO    ] [             ]  Confidential unpublished
data - All rights reserved
2022-01-07 12:28:30.408357 [INFO    ] [syn1588      ]  Syn1588Ifc requires at
least:
2022-01-07 12:28:30.408384 [INFO    ] [syn1588      ]  - linux driver version 1.4-
15-g05b7283
2022-01-07 12:28:30.408404 [INFO    ] [syn1588      ]  - windows driver version
10/05/2017, 10.9.16.182
2022-01-07 12:28:30.408451 [INFO    ] [syn1588      ]  Device /dev/syncD0 found
2022-01-07 12:28:30.408503 [INFO    ] [syn1588      ]  syn1588(R) Hardware Clock M
2.3.5 f=125000000 Hz
2022-01-07 12:28:30.408535 [INFO    ] [syn1588      ]  Found stop clock support
2022-01-07 12:28:30.408572 [INFO    ] [syn1588      ]  Using MAC TS Version 3160
2022-01-07 12:28:30.408595 [INFO    ] [syn1588      ]  Using programmable 1-step
TS
Selected syn1588(R) card 0
```

After identifying your card number quit the syn1588 utility by using the “quit” command. Use command “ifconfig” to find out the Ethernet interface of your syn1588®PCIe NIC by comparing the MAC addresses. In our example it is “eth1”.

Caution:

Do not invoke the syn1588 utility after starting the vSync utility as the former initializes the Jitter Cleaner PLL which causes the PLL to loose lock. One may start the syn1588 utility in a separate shell and keep it open for purposes like re-configuring the IOMATRIX register etc.

```
root@ubuntu:/opt/oregano# ifconfig
eth0      Link encap:Ethernet  HWaddr d0:50:99:2a:ef:05
          inet addr:192.168.102.192  Bcast:192.168.103.255
          inet6 addr: fe80::d250:99ff:fe2a:ef05/64 Scope:Link
          UP BROADCAST RUNNING MULTICAST  MTU:1500  Metric:1
          RX packets:18962 errors:0 dropped:0 overruns:0 frame:0
          TX packets:115 errors:0 dropped:0 overruns:0 carrier:0
          collisions:0 txqueuelen:1000
          RX bytes:3203506 (3.2 MB)  TX bytes:16051 (16.0 KB)

eth1      Link encap:Ethernet  HWaddr 8c:a5:a1:00:00:6b
          inet6 addr: fe80::8ea5:a1ff:fe00:6b/64 Scope:Link
          UP BROADCAST RUNNING MULTICAST  MTU:1500  Metric:1
          RX packets:5235 errors:0 dropped:0 overruns:0 frame:0
          TX packets:875 errors:0 dropped:0 overruns:0 carrier:63
          collisions:0 txqueuelen:1000
          RX bytes:471150 (471.1 KB)  TX bytes:13371102 (13.3 MB)
          Interrupt:16 Memory:90700000-90710000

lo        Link encap:Local Loopback
          inet addr:127.0.0.1  Mask:255.0.0.0
          inet6 addr: ::1/128 Scope:Host
          UP LOOPBACK RUNNING  MTU:65536  Metric:1
          RX packets:163 errors:0 dropped:0 overruns:0 frame:0
          TX packets:163 errors:0 dropped:0 overruns:0 carrier:0
          collisions:0 txqueuelen:0
          RX bytes:11774 (11.7 KB)  TX bytes:11774 (11.7 KB)
```

Step 2: Start syn1588® PTP Stack

Open a syn1588 shell and start the syn1588® PTP Stack by using the command "./ptp". Add the parameters "-i eth1" (interface identified in Step 1), "-C M_EXT" (Master on external reference), "-d 0" (Domain 0..255, default Domain is 0) and optional "-v 2" (loglevel 2 includes errors and warnings).

Alternatively if you want to run the syn1588® PTP Stack in other configuration for example as slave please choose one of your appreciated parameter:

-C options set Clock Class (0..255)

M_EXT....Master on external reference

M_HOLD...Master on external reference (in holdover)

M_NSYNC..Master on external reference (not sync'd)

M_SLAVE..Master on external reference (may be Slave)

S...Slave only

Figure 9 Open syn1588 shell

```
oregano@KAEFER:/opt/oregano/bin$ sudo ./ptp -i enp2s0 -C M_EXT -d 20 -v info
2022-01-07 12:31:12.562888 [INFO    ] [             ]  syn1588(R) PTP Stack -
IEEE1588-2008 Engine
2022-01-07 12:31:12.562922 [INFO    ] [             ]  Build date: 2022-01-
05T12:43:16 - v1.14-9-g7cbf9e73
2022-01-07 12:31:12.562927 [INFO    ] [             ]  Copyright (c) Oregano
Systems - Design & Consulting GesmbH 2005-2022
2022-01-07 12:31:12.562932 [INFO    ] [             ]  Confidential unpublished
data - All rights reserved
```

```
2022-01-07 12:31:12.562939 [INFO    ] [             ]  syn1588(R) PTP Stack
started: 2022-01-07 11:31:12.562937 (UTC)
2022-01-07 12:31:12.563036 [INFO    ] [p1           ]  Port 1: adding config "i" =
"enp2s0"
2022-01-07 12:31:12.563046 [INFO    ] [p1           ]  Port 1: adding config "C" =
"M_EXT"
2022-01-07 12:31:12.563051 [INFO    ] [p1           ]  Port 1: adding config "d" =
"20"
2022-01-07 12:31:12.563057 [INFO    ] [p1           ]  Port 1: adding config "v" =
"info"
2022-01-07 12:31:12.563063 [INFO    ] [p1           ]  PTP version 2.0
2022-01-07 12:31:12.563068 [INFO    ] [             ]  Command line: ./ptp -i
enp2s0 -C M_EXT -d 20 -v info
2022-01-07 12:31:12.563083 [WARNING ] [             ]  Failed to set high priority
for the PTP thread!
2022-01-07 12:31:12.563094 [INFO    ] [p1           ]  Found Configuration for 1
ports
2022-01-07 12:31:12.563328 [INFO    ] [syn1588      ]  Syn1588Ifc requires at
least:
2022-01-07 12:31:12.563337 [INFO    ] [syn1588      ]  - linux driver version 1.4-
15-g05b7283
2022-01-07 12:31:12.563342 [INFO    ] [syn1588      ]  - windows driver version
10/05/2017, 10.9.16.182
2022-01-07 12:31:12.563356 [INFO    ] [syn1588      ]  Device /dev/syncD0 found
2022-01-07 12:31:12.563373 [INFO    ] [syn1588      ]  syn1588(R) Hardware Clock M
2.3.5 f=125000000 Hz
2022-01-07 12:31:12.563382 [INFO    ] [syn1588      ]  Found stop clock support
2022-01-07 12:31:12.563394 [INFO    ] [syn1588      ]  Using MAC TS Version 3160
2022-01-07 12:31:12.563399 [INFO    ] [syn1588      ]  Using programmable 1-step
TS
2022-01-07 12:31:12.563431 [INFO    ] [syn1588      ]  syn1588(R) PCIe NIC
Revision 2, Build 865
2022-01-07 12:31:12.563448 [INFO    ] [p1           ]  Using syn1588 mode
2022-01-07 12:31:12.563477 [INFO    ] [p1.clock     ]  Spike M2S: Init with ival
0, buffer size 16
2022-01-07 12:31:12.563554 [INFO    ] [p1.clock     ]  Spike Path: Init with ival
0, buffer size 16
2022-01-07 12:31:12.563570 [INFO    ] [p1.io        ]  Init shared mem
2022-01-07 12:31:12.565766 [INFO    ] [syn1588      ]  syn1588HwClk: clearing leap
second jump
2022-01-07 12:31:12.565777 [INFO    ] [p1.engine    ]  Settings: ClockId
00:1e:c0:ff:fe:85:de:2b
2022-01-07 12:31:12.565784 [INFO    ] [p1.engine    ]  Settings: Prio1 128
ClkClass 6 clkAccuracy 39 clkVariance 65535
2022-01-07 12:31:12.565791 [INFO    ] [p1.engine    ]  Settings: Prio2 128 Domain
20
2022-01-07 12:31:12.565919 [INFO    ] [p1.network.mcport]  SIOCSHWTSTAMP: tx_type
1 requested, got 1; rx_filter 0 requested, got 12
2022-01-07 12:31:12.565930 [INFO    ] [p1.network.mcport]  Activated
SO_TIMESTAMPING hardware
2022-01-07 12:31:12.566027 [INFO    ] [p1.network.mcport]  SIOCSHWTSTAMP: tx_type
1 requested, got 1; rx_filter 0 requested, got 12
2022-01-07 12:31:12.566036 [INFO    ] [p1.network.mcport]  Activated
SO_TIMESTAMPING hardware
2022-01-07 12:31:12.566299 [INFO    ] [p1.clock     ]  Clk: Using Oregano Systems;
syn1588(R) PCIe NIC Revision 2; 00:1E:C0:85:DE:2B
2022-01-07 12:31:12.566308 [INFO    ] [p1.clock     ]    with ClockId
00:1e:c0:ff:fe:85:de:2b
2022-01-07 12:31:12.566445 [INFO    ] [p1.clock     ]  Clk: Resetting servos
2022-01-07 12:31:12.566450 [INFO    ] [p1.clock     ]  Clk: Resetting filters
2022-01-07 12:31:12.566456 [INFO    ] [p1.clock     ]  Spike M2S: Init with ival
0, buffer size 16
2022-01-07 12:31:12.566462 [INFO    ] [p1.clock     ]  Spike Path: Init with ival
0, buffer size 16
2022-01-07 12:31:12.566472 [INFO    ] [p1.io        ]  Init shared mem
2022-01-07 12:31:12.566485 [INFO    ] [syn1588      ]  syn1588HwClk: clearing leap
second jump
```

```
2022-01-07 12:31:12.566510 [INFO    ] [p1.engine    ]  1641555109.567559456s State
Listening
2022-01-07 12:31:13.566518 [INFO    ] [p1.engine    ]  State Change Initializing -
> Listening
2022-01-07 12:31:13.566614 [INFO    ] [syn1588      ]  syn1588HwClk: UTC offset
changed to 37 s
2022-01-07 12:31:13.566686 [INFO    ] [p1.engine    ]  1641555110.567732391s State
Listening
2022-01-07 12:31:14.566828 [INFO    ] [p1.engine    ]  1641555111.567874086s State
Listening
2022-01-07 12:31:15.567119 [INFO    ] [p1.engine    ]  1641555112.568164630s State
Listening
2022-01-07 12:31:16.567924 [INFO    ] [p1.engine    ]  1641555113.568970336s State
Listening
2022-01-07 12:31:17.568208 [INFO    ] [p1.engine    ]  1641555114.569253496s State
Listening
2022-01-07 12:31:18.568494 [INFO    ] [p1.engine    ]  1641555115.569540160s State
Listening
2022-01-07 12:31:19.568778 [INFO    ] [p1.engine    ]  1641555116.569823408s State
Listening
2022-01-07 12:31:19.745195 [INFO    ] [p1.engine    ]  State Change Listening ->
Master
2022-01-07 12:31:19.745271 [INFO    ] [p1.engine    ]  <--- Announce seqId: 1
2022-01-07 12:31:19.745470 [INFO    ] [p1.engine    ]  <--- Sync seqId: 1
2022-01-07 12:31:19.745684 [INFO    ] [p1.engine    ]  <--- FollowUp seqId: 1
2022-01-07 12:31:20.569310 [INFO    ] [p1.engine    ]  1641555117.570355113s State
Master
2022-01-07 12:31:20.569438 [INFO    ] [p1.engine    ]  <--- Announce seqId: 2
2022-01-07 12:31:20.745732 [INFO    ] [p1.engine    ]  <--- Sync seqId: 2
2022-01-07 12:31:20.745878 [INFO    ] [p1.engine    ]  <--- FollowUp seqId: 2
2022-01-07 12:31:21.569849 [INFO    ] [p1.engine    ]  1641555118.570879690s State
Master
2022-01-07 12:31:21.746256 [INFO    ] [p1.engine    ]  <--- Sync seqId: 3
2022-01-07 12:31:21.746432 [INFO    ] [p1.engine    ]  <--- FollowUp seqId: 3
2022-01-07 12:31:22.570358 [INFO    ] [p1.engine    ]  1641555119.571403875s State
Master
```

Step 3: Start vSync utility with digital mode

Open a syn1588 shell and start the syn1588 vsync utility by using the command "./vsync". Add the parameters "-d 0" (card number identified in step 1), choose the selected video mode using "-m 625i" (for this example the video mode ST170 PAL interlaced, 25Hz), "-t digital" to request digital sync signal output and optionally define a verbosity level for the output by "-v 2" (loglevel 2 includes errors and warnings). One can also redirect the log output to a file using the "-f filename" command line option.

Figure 10 Open syn1588 shell

```
oregano@KAEFER:/opt/oregano/bin$ sudo ./vSync -d 0 -m 625i -t digital -v info
2022-01-07 12:43:19.135354 [INFO    ] [             ]  syn1588(R) vSync - Video
Synchronization Engine
2022-01-07 12:43:19.135386 [INFO    ] [             ]  Build date: 2022-01-
05T12:43:16 - v1.14-9-g7cbf9e73
2022-01-07 12:43:19.135391 [INFO    ] [             ]  Copyright (c) Oregano
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2022-01-07 12:43:19.135396 [INFO    ] [             ]  Confidential unpublished
data - All rights reserved
2022-01-07 12:43:19.135401 [INFO    ] [             ]  Command line: ./vSync -d 0
-m 625i -t digital -v info
2022-01-07 12:43:19.135424 [INFO    ] [             ]  Port 0: adding config "d" =
"0"
2022-01-07 12:43:19.135433 [INFO    ] [             ]  Port 0: adding config "m" =
"625i"
2022-01-07 12:43:19.135438 [INFO    ] [             ]  Port 0: adding config "t" =
"digital"
2022-01-07 12:43:19.135444 [INFO    ] [             ]  Port 0: adding config "v" =
"info"
2022-01-07 12:43:19.135454 [INFO    ] [syn1588      ]  Syn1588Ifc requires at
least:
2022-01-07 12:43:19.135460 [INFO    ] [syn1588      ]  - linux driver version 1.4-
15-g05b7283
2022-01-07 12:43:19.135465 [INFO    ] [syn1588      ]  - windows driver version
10/05/2017, 10.9.16.182
2022-01-07 12:43:19.135485 [INFO    ] [syn1588      ]  Device /dev/syncD0 found
2022-01-07 12:43:19.135519 [INFO    ] [syn1588      ]  syn1588(R) Hardware Clock M
2.3.5 f=125000000 Hz
2022-01-07 12:43:19.135531 [INFO    ] [syn1588      ]  Found stop clock support
2022-01-07 12:43:19.135542 [INFO    ] [syn1588      ]  Using MAC TS Version 3160
2022-01-07 12:43:19.135547 [INFO    ] [syn1588      ]  Using programmable 1-step
TS
2022-01-07 12:43:19.135566 [INFO    ] [syn1588      ]  syn1588(R) PCIe NIC
Revision 2, Build 865
2022-01-07 12:43:19.135597 [INFO    ] [1.sharedmemory.api.io]  Init shared mem
2022-01-07 12:43:22.503184 [INFO    ] [Main         ]  Video Processing started
2022-01-07 12:43:22.503500 [INFO    ] [Main.SDIAudio]  Starting SDI counter at the
next full second 1641555840
```

```
2022-01-07 12:43:22.503533 [INFO    ] [Main.SDIAudio]  SDI 27 MHz counter:
2474614784
2022-01-07 12:43:22.503557 [INFO    ] [Main.SDIAudio]  SDI 90 kHz counter:
1740552192
2022-01-07 12:43:22.503654 [INFO    ] [Main.SDIAudio]  Starting Video Signal
generation for video mode 625i
2022-01-07 12:43:22.504013 [INFO    ] [Main         ]  starting generation of
video signals at time: 1641555839.501087900
2022-01-07 12:43:22.504037 [INFO    ] [Main         ]  HSYNC & FrameSYNC signals
are digitally generated by the FPGA
2022-01-07 12:43:22.504056 [INFO    ] [Main         ]  Period0 is provided on SMA
X7 and FrameSYNC on SMA X6
```

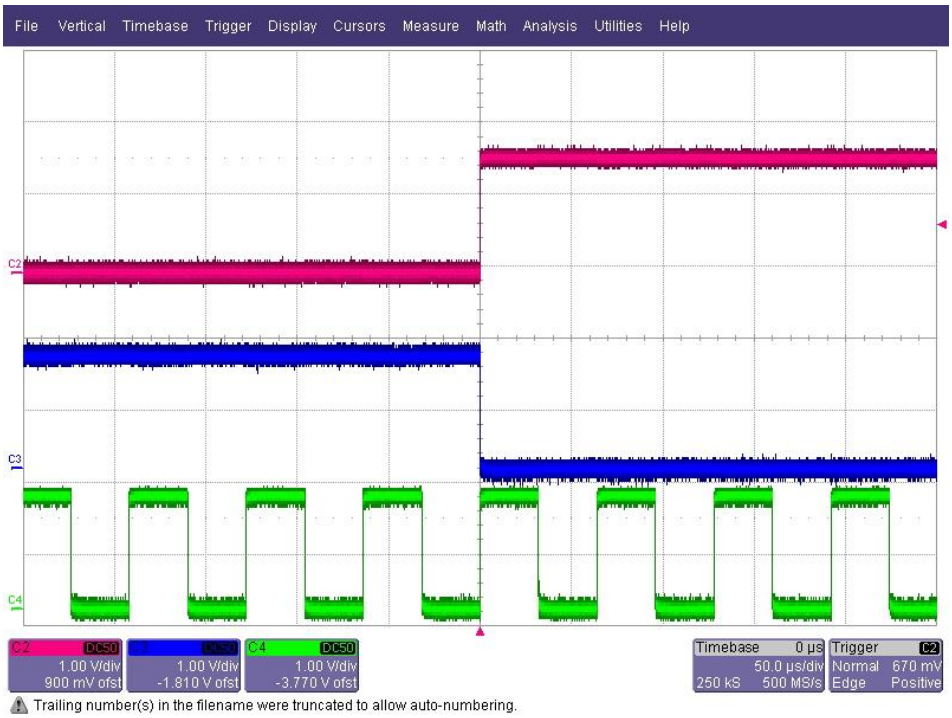

Figure 11 Digital Video Mode 625i (master operation)

Figure 11 shows the digital frame sync signal (channel 3 / blue) for the digital video Mode 625i, the 1 PPS signal from the syn1588® PCIe NIC (channel 2 / red) and the Period 0 signal (channel 4 / green). One may configure the GENLOCKCTRL register (as defined in an_register_map.pdf), to output HSYNC signal instead of Period0 signal. The frame sync signal is perfectly phase locked to the 1 PPS master reference signal. One can use the oscilloscope or any video test equipment to verify this behavior.

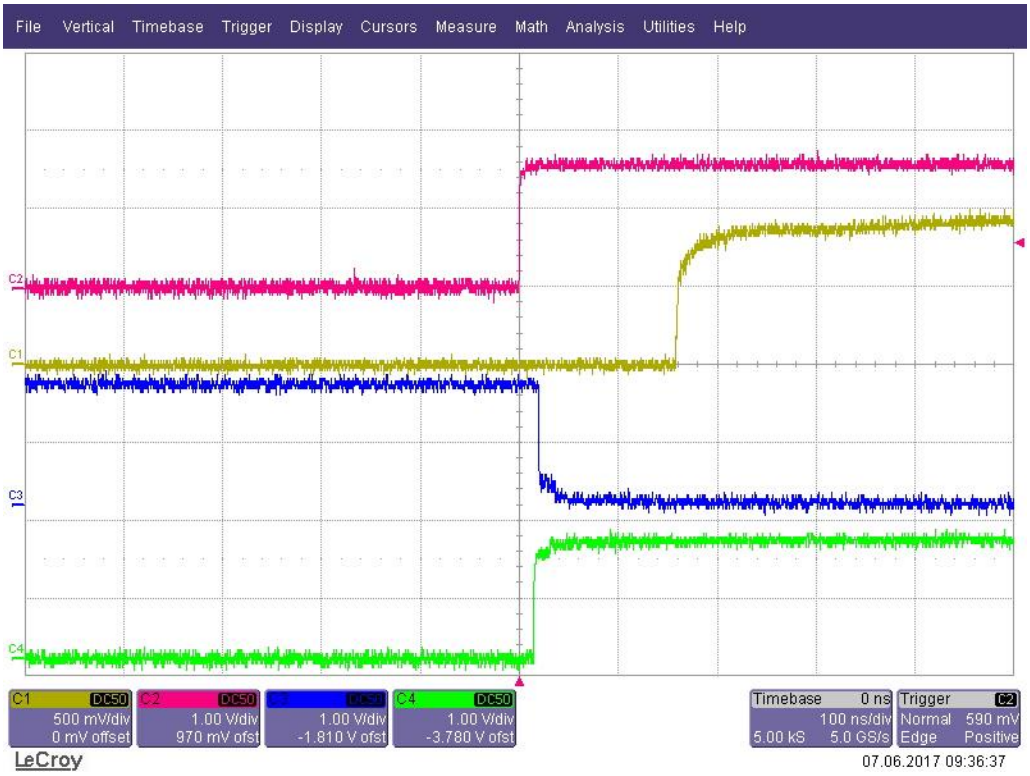

Figure 12 Digital Video Mode 625i (slave operation) – detail view

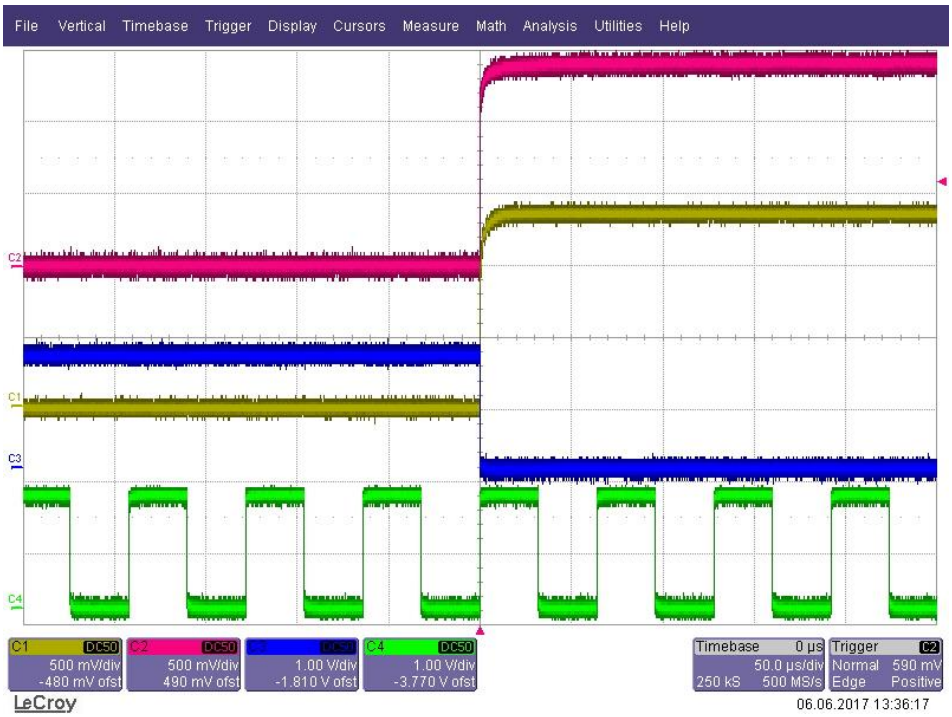

Figure 13 Mode 625i (slave operation) – overview

Figure 12 shows the 1PPS reference signal from the master (channel 1 / yellow), the local 1PPS signal (channel 2 / yellow), the digital frame sync signal (channel 3 / blue) for the digital video Mode 625i for the digital video Mode 625i and the PERIOD0 signal (channel 4 / green). One may configure the card to output HSYNC signal instead of PERIOD0 signal. Please contact Oregano Systems support if you require this mode.

The syn1588® PCIe NIC acts as slave and is synchronized to the master reference. The frame sync signal is phase locked to the 1 PPS of the Grandmaster in the network. The jitter between the 1 PPS of Grandmaster signal and the generated frame sync signal depends on the clock synchronization accuracy. The delay between the 1 PPS of master and slave is due to the cable delay from the 1 PPS output of the master and the oscilloscope. While Figure 12 shows a detailed view allowing to analyse the offset, Figure 13 shows the overview of the signals (the big picture).

Literature

AN002. (Version 2.8 - March 2019). *Application Note: "Ordering syn1588® PCIe NIC Revsion 2.1".* Oregano Systems.

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