



Version 1.21 – March 2019

Features

- IEEE1588-2008 1-step end-2-end transparent clock
- Hardware time stamping with 2 nsec resolution
- Residence time measurement accuracy better than 500ps (σ)
- Support for IEEE1588 layer-2 and layer-3 communication
- Fully hardware based PTP packet processing
- On-the-fly time stamping using patented 1-step technology
- Capable of handling high packet rates (>64/sec) simultaneously on all ports
- Low latency for PTP packets
- PTP - VLAN support
- PTP - IPv6 support
- Remote PTP monitoring and configuration via SNMP
- Local oscillator options
 - TCXO
 - OCXO
- 8+1 port 10/100/1000 Mbit Ethernet switch following IEEE802.3-2005
- 9th port offers SFP cage
 - Fiber 1000Base-X
 - Copper 1000Base-T
- Wide range AC power supply included on-board
- 19" 1HE rackmount case



syn1588[®] Gbit Switch 8+1 Port

Highly accurate clock synchronization systems profit from IEEE1588 aware Ethernet switches to overcome unpredictable delay variations introduced by standard Ethernet switches as a consequence of varying network load conditions.

The syn1588[®] Gbit Ethernet Switch offers a simple plug & play solution to this problem by implementing 1-step end-2-end transparent clock functionality with respect to IEEE1588-2008 using Oregano Systems' patented on-the-fly time stamping technology.

Owing to the fact that the complete PTP packet processing is implemented exclusively in hardware; the residence time of PTP event packets is not affected remaining in the range of 2 μ s.

All time stamps are drawn at a resolution of 2 ns yielding accuracies of 500 ps (σ) for measuring the residence time of any IEEE 1588-2008 event message (sync, del_req, p_del_req, and p_del_resp) In combination with highly accuracy PTP end nodes (such as syn1588[®] devices by Oregano Systems equipped with OCXOs) an overall synchronization accuracy of less than 5 ns may be achieved independently of the network load condition.

The syn1588[®] Gbit Switch supports time stamping of all PTP event messages encapsulated in VLAN as well as Ethernet (PTP layer-2), IPV4, and IPV6.

The syn1588[®] Gbit Switch is a triple speed 8 port layer-2 Ethernet switch with an additional up-link port. This port is equipped with an SFP-type interface allowing either a copper or a fiber optic communication link to be installed.

As the IEEE1588 event packet processing is implemented purely in hardware the syn1588[®] Gbit Switch is capable of handling high message rates of more than 64 messages simultaneously on all incoming and outgoing ports.

The syn1588[®] Gbit Switch may be ordered with different oscillator options ranging from simple 50 ppm XOs to TCXOs and even OCXOs. The latter will provide sub-ns accuracy for any time stamping done by the syn1588[®] Gbit Switch.

Remote management as well as monitoring and configuration of all PTP functions is realized via SNMP.



syn1588®

syn1588® Gbit Switch

1-step end2end Transparent Clock

Brief Data Sheet

Version 1.21 – March 2019

Technical Specifications	
Standards	IEEE802.3-2005 IEEE1588-2008
Storage temperature	-40°C to 85°C
Operating temperature	0°C to 50°C
Humidity	5% to 90% non-condensing
Dimension	Height: 43,6mm (1HE); Depth: 254mm; Installation width: 444mm
Weight	3,73 kg



Franzosengraben 8
A-1030 Vienna
Austria
<http://oregano.at>
contact@oregano.at

Copyright © 2019

Oregano Systems – Design & Consulting GmbH

ALL RIGHTS RESERVED.

Oregano Systems does not assume any liability arising out of the application or use of any product described or shown herein nor does it convey any license under its patents, copyrights, or any rights of others.

Licenses or any other rights such as, but not limited to, patents, utility models, trademarks or tradenames, are neither granted nor conveyed by this document, nor does this document constitute any obligation of the disclosing party to grant or convey such rights to the receiving party.

Oregano Systems reserves the right to make changes, at any time without notice, in order to improve reliability, function or design. Oregano Systems will not assume responsibility for the use of any circuitry described herein.

All trademarks used in this document are the property of their respective owners.