

Determining the PHY delay of syn1588® products

Version 1.11 - December 2021

Abstract

This application describes the calculation of the PHY delay values for the $syn1588^{\circ}$ Gbit Switch and $syn1588^{\circ}$ PCle NIC. The $syn1588^{\circ}$ Dual NIC uses the identical PHY delay values (for both network interfaces) as the $syn1588^{\circ}$ PCle NIC – SFP version.

The receive PHY delay will be automatically subtracted from the receive timestamp while the transmit PHY delay will be added to the transmit timestamp drawn by the respective syn1588® timestamping units.

syn1588® Gbit Switch

RX PHY Delay

The timestamp is drawn following a 3-stage synchronizer engine running at 125 MHz (i.e. 8 ns) resulting in a delay of 2,5 periods (i.e. 20 ns) on the average. This value has to be subtracted from the timestamp drawn.

Additionally the Marvell PHY adds a delay that need to be subtracted from the timestamp drawn.

GMII	Description	t [ns]
	timestamper synchronizer stage	-20
	input delay 3 clocks	-24
	PHY delay	-191
	RX PHY delay register value	-235
MII	Description	t [ns]
	timestamper synchronizer stage	-20
	input delay 7 clocks	-280
	PHY delay	-229
	RX PHY delay register value	-529

TX PHY Delay

There is one clock delay while sending the data to the PHY. This value has to be added to the timestamp drawn.

The timestamp is drawn following a 3-stage synchronizer engine running at 125 MHz (i.e. 8 ns) resulting in a delay of 2,5 periods (i.e. 20 ns) on the average. This value has to be subtracted from the timestamp drawn.

Additionally the (Marvell) PHY adds a delay that need to be added to the timestamp drawn.

GMII	Description	t [ns]
	output register 1 gmii clock at port_handling	8
	timestamper synchronizer stage	-20
	PHY delay	122
	total delay	110
MII	Description	t [ns]
	output register 1 mii clock at port_handling	40
	timestamper synchronizer stage	-20
	PHY delay	116
	total delay	136

RX PHY Delay (Build 115 and newer)

The timestamp is drawn following a 3-stage synchronizer engine running at 125 MHz (i.e. 8 ns) resulting in a delay of 2,5 periods (i.e. 20 ns) on the average. This value has to be subtracted from the timestamp drawn.

Additionally the (Marvell) PHY adds a delay that need to be subtracted from the timestamp drawn.

GMII	Description	t [ns]
	timestamper synchronizer stage	-20
	input delay 1 clocks	-8
	PHY delay	-191
	RX PHY delay register value	-219
MII	Description	t [ns]
	timestamper synchronizer stage	-20
	input delay 3 clocks	-120
	PHY delay	-229
	RX PHY delay register value	-369

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TX PHY Delay (Build 115 and newer)

Starting with firmware build version 115 a modified timestamping structure is used resulting in a different delay behavior.

GMII	Description	t [ns]
	output delay	136
	timestamper synchronizer stage	-20
	PHY delay	122
	total delay	238
MII	Description	t [ns]
	output delay	1360
	timestamper synchronizer stage	-20
	PHY delay	116
	total delay	1456

syn1588® PCIe NIC - Board Revision 1.5

RX PHY Delay

There are two input registers in the receive MAC resulting in a delay of 16 ns for GMII or 80 ns for MII. This value has to be subtracted from the timestamp drawn.

The timestamp is drawn following a 3-stage synchronizer engine running at 87,5 MHz (i.e. 11.43 ns) resulting in a delay of 2,5 periods (i.e. 28,57 ns) on the average. Two stages of the synchronizer are compensated within the syn1588® Clock_M IP core resulting in a delay of 5,72 ns. This value has to be subtracted from the timestamp drawn.

Additionally the Marvell PHY 88E1111 adds a delay that need to be subtracted from the timestamp drawn.

GMII	Description	t [ns]
	input registers	-16
	timestamper synchronizer stage	-29
	average compensated timestamper synchronizer delay	-6
	PHY device delay	-191
	PHY delay register value	-213
MII	Description	t [ns]
	input register	-80
	timestamper synchronizer stage	-6
	PHY device delay	-229
	PHY delay register value	-315

TX PHY Delay

There is one output register for GMII (i.e. 8 ns) in the unit topcore and one clock delay while sending the data to the PHY resulting in a delay of 16 ns for GMII or 80 ns for MII. This value has to be added to the timestamp drawn.

The timestamp is drawn following a 3-stage synchronizer engine running at 87,5 MHz (i.e. 11.43 ns) resulting in a delay of 2,5 periods (i.e. 28,57 ns) on the average. Two stages of the synchronizer are compensated within the syn1588® Clock_M IP core resulting in a delay of 5,72 ns. This value has to be subtracted from the timestamp drawn.

Additionally the Marvell PHY 88E1111 adds a delay that need to be added to the timestamp drawn.

GMII	Description	t [ns]
	output register & TX delay	16
	timestamper synchronizer stage	-29
	average compensated timestamper synchronizer delay	-6
	PHY device delay	122
	PHY delay register value	132
MII	Description	t [ns]
	output register & TX delay	80
	timestamper synchronizer stage	-29
	average compensated timestamper synchronizer delay	-6
	PHY device delay	116
	PHY delay register value	190

syn1588® PCIe NIC - Board Revision 2.x

RX PHY Delay

There are three input registers in the receive MAC resulting in a delay of 24 ns for GMII or 120 ns for MII. This value has to be subtracted from the timestamp drawn.

The timestamp is drawn following a 3-stage synchronizer engine running at 125 MHz (i.e. 8 ns) resulting in a delay of 2,5 periods (i.e. 20 ns) on the average. Two stages of the synchronizer are compensated within the syn1588® Clock_M IP core resulting in a delay of 4 ns. This value has to be subtracted from the timestamp drawn.

Additionally the PHY (Micrel KSZ9031) adds a delay that need to be subtracted from the timestamp drawn. The PHY delay register value is the same at TSE_MAC and syn1588[®]Clock_M RX time-stampers.

GMII	Description	t [ns]
	input registers	-24
	timestamper synchronizer stage	-20
	average compensated timestamper synchronizer delay	-4
	PHY device delay	-359
	PHY delay register value	-387
MII	Description	t [ns]
	input register	-120
	timestamper synchronizer stage	-20
	average compensated timestamper synchronizer delay	-4
	PHY device delay	-445
	PHY delay register value	-569

TX PHY Delay

There is one output register for GMII (i.e. 8 ns) and one clock delay while sending the data to the PHY resulting in a delay of 16 ns for GMII or 80 ns for MII. This value has to be added to the timestamp drawn. In addition, there is one output register while sending the transmit data from the MAC to the syn1588®Clock_M. This means an additional period of GMII/MII (8 ns/40 ns) clock period has to the added to the PHY delay register of the MAC timestamper but it is not to be added for that of the syn1588®Clock_M transmit time-stamper.

The timestamp is drawn following a 3-stage synchronizer engine running at 125 MHz (i.e. 8 ns) resulting in a delay of 2,5 periods (i.e. 20 ns) on the average. Two stages of the synchronizer are compensated within the syn1588® Clock_M IP core resulting in a delay of 4 ns. This value has to be subtracted from the timestamp drawn.

Additionally the PHY (Micrel KSZ9031) adds a delay that need to be added to the timestamp drawn.

GMII	Description	t [ns]
	output register & TX delay	16
	additional output register from TX_MAC to CLOCK_M	8
	timestamper synchronizer stage	-20
	average compensated timestamper synchronizer delay	-4
	PHY device delay	135
	PHY delay register value CLOCK_M	147
	PHY delay register value TX_MAC	155
MII	Description	t [ns]
	output register & TX delay	80
	additional output register from TX_MAC to CLOCK_M	40
	timestamper synchronizer stage	-20
	average compensated timestamper synchronizer delay	-4
	PHY device delay	166
	PHY delay register value CLOCK_M	242
	PHY delay register value TX_MAC	282

syn1588[®] PCIe NIC – SFP Version (Rev 2.1)

RX PHY Delay: Fiber Transceiver Module

There are three input registers in the receive MAC resulting in a delay of 24 ns for GMII. This value has to be subtracted from the timestamp drawn.

The timestamp is drawn following a 3-stage synchronizer engine running at 125 MHz (i.e. 8 ns) resulting in a delay of 2,5 periods (i.e. 20 ns) on the average. Two stages of the synchronizer are compensated within the syn1588® Clock_M IP core resulting in a delay of 4 ns. This value has to be subtracted from the timestamp drawn.

Additionally, the PCS/PMA unit as well as the clock crossing FIFO (5.5 clocks on the average) after the MAC adds a delay that need to be subtracted from the timestamp drawn. The PHY delay register value is the same at TSE_MAC and syn1588®Clock_M RX time-stampers.

GMII	Description	t [ns]
	input registers	-24
	timestamper synchronizer stage	-20
	average compensated timestamper synchronizer delay	-4
	clock crossing FIFO	-44
	PCS/PMA delay	-48
	PHY delay register value	-140

TX PHY Delay: Fiber Transceiver Module

There is one output register for GMII (i.e. 8 ns) and one clock delay while sending the data to the PHY resulting in a delay of 16 ns for GMII. This value has to be added to the timestamp drawn. In addition, there is one output register while sending the transmit data from the MAC to the syn1588®Clock_M. This means an additional period of GMII (8 ns) clock period has to the added to the PHY delay register of the MAC time-stamper but it is not to be added for that of the syn1588®Clock_M transmit time-stamper.

The timestamp is drawn following a 3-stage synchronizer engine running at 125 MHz (i.e. 8 ns) resulting in a delay of 2,5 periods (i.e. 20 ns) on the average. Two stages of the synchronizer are compensated within the syn1588® Clock_M IP core resulting in a delay of 4 ns. This value has to be subtracted from the timestamp drawn.

Additionally, the PCS/PMA unit as well as the clock crossing FIFO (5.5 clocks on the average) in front of the MAC adds a delay that need to be added to the timestamp drawn.

GMII	Description	t [ns]
	output register & TX delay	16
	additional output register from TX_MAC to CLOCK_M	8
	timestamper synchronizer stage	-20
	average compensated timestamper synchronizer delay	-4
	clock crossing FIFO	44
	PCS/PMA delay	8
	PHY delay register value CLOCK_M	44
	PHY delay register value TX_MAC	52

RX PHY Delay: Copper Transceiver Module

There are three input registers in the receive MAC resulting in a delay of 24 ns for GMII or 120 ns for MII. This value has to be subtracted from the timestamp drawn.

The timestamp is drawn following a 3-stage synchronizer engine running at 125 MHz (i.e. 8 ns) resulting in a delay of 2,5 periods (i.e. 20 ns) on the average. Two stages of the synchronizer are compensated within the syn1588® Clock_M IP core resulting in a delay of 4 ns. This value has to be subtracted from the timestamp drawn.

Additionally the PCS/PMA unit as well as the clock crossing FIFO (5.5 clocks on the average) after the MAC and the PHY in the SFP transceiver module adds a delay that need to be subtracted from the timestamp drawn. The PHY delay register value is the same at TSE_MAC and syn1588®Clock_M RX timestampers.

GMII	Description	t [ns]
	input registers	-24
	timestamper synchronizer stage	-20
	average compensated timestamper synchronizer delay	-4
	clock crossing FIFO	-44
	PCS/PMA delay	-143
	PHY device delay	-272
	PHY delay register value	-507
MII	Description	t [ns]
	input register	-120
	timestamper synchronizer stage	-20
	average compensated timestamper synchronizer delay	-4
	clock crossing FIFO	-220
	PCS/PMA delay	-215
	PHY device delay	-272
	PHY delay register value	-851

TX PHY Delay: Copper Transceiver Module

There is one output register for GMII (i.e. 8 ns) and one clock delay while sending the data to the PHY resulting in a delay of 16 ns for GMII or 80 ns for MII. This value has to be added to the timestamp drawn. In addition, there is one output register while sending the transmit data from the MAC to the syn1588®Clock_M. This means an additional period of GMII/MII (8 ns/40 ns) clock period has to the added to the PHY delay register of the MAC timestamper but it is not to be added for that of the syn1588®Clock_M transmit time-stamper.

The timestamp is drawn following a 3-stage synchronizer engine running at 125 MHz (i.e. 8 ns) resulting in a delay of 2,5 periods (i.e. 20 ns) on the average. Two stages of the synchronizer are compensated within the syn1588® Clock_M IP core resulting in a delay of 4 ns. This value has to be subtracted from the timestamp drawn.

Additionally the PCS/PMA as well as the clock crossing FIFO (5.5 clocks on the average) in front of the MAC and the PHY in the SFP transceiver module unit adds a delay that need to be added to the timestamp drawn.

GMII	Description	t [ns]
	output register & TX delay	16
	additional output register from TX_MAC to CLOCK_M	8
	timestamper synchronizer stage	-20
	average compensated timestamper synchronizer delay	-4
	clock crossing FIFO	44
	PCS/PMA delay	104
	PHY device delay	280
	PHY delay register value CLOCK_M	420
	PHY delay register value TX MAC	428
MII	Description	t [ns]
	•	- []
	output register & TX delay	80
	•	
	output register & TX delay additional output register from	80
	output register & TX delay additional output register from TX_MAC to CLOCK_M	80 40
	output register & TX delay additional output register from TX_MAC to CLOCK_M timestamper synchronizer stage average compensated	80 40 -20
	output register & TX delay additional output register from TX_MAC to CLOCK_M timestamper synchronizer stage average compensated timestamper synchronizer delay	80 40 -20 -4
	output register & TX delay additional output register from TX_MAC to CLOCK_M timestamper synchronizer stage average compensated timestamper synchronizer delay clock crossing FIFO	80 40 -20 -4 220
	output register & TX delay additional output register from TX_MAC to CLOCK_M timestamper synchronizer stage average compensated timestamper synchronizer delay clock crossing FIFO PCS/PMA delay	80 40 -20 -4 220 376

Summary

This application note described the calculation of the PHY delay correction values.



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