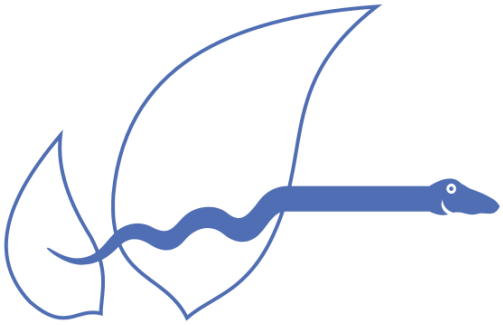

syn1588 ®

syn1588® enabled IEEE 1588 compliant clock synchronisation

syn1588® Clock_M IP Core Family

Data Sheet

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1.1 Contents

1.2 List of Figures

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2 Overview

Oregano Systems' syn1588® Clock_M IP cores provides highly accurate clock synchronization functions compliant to the IEEE1588 standards 2002 and 2008. The syn1588® Clock_M IP cores holds all required hardware functions for efficiently implementing a high-accuracy, high-performance IEEE1588 node. The IP core is made up of the following four major function blocks:

- CPU interface
- High-precision hardware clock with clock control
- Network timestamping units
- Signal Generation

The following architectural block diagram shows the overview of the syn1588® Clock_M IP core.

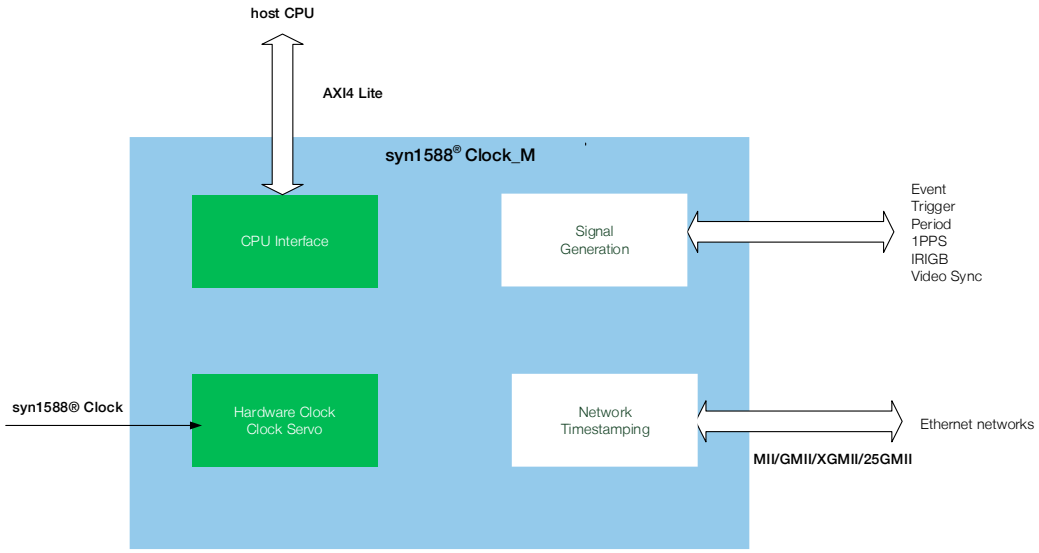

Figure 1: syn1588® Clock_M basic block diagram

The syn1588® Clock_M IP core is available in different flavours.

- syn1588® Clock_M … single network 100/1000 Mbit interface
- syn1588® Clock_MX … multiple network 100/1000 Mbit interface
- syn1588® Clock_M_10G … single network 10 Gbit interface
- syn1588® Clock_MX_10G … multiple network 10 Gbit interfaces
- syn1588® Clock_M_25G … single network 25 Gbit interface
- syn1588® Clock_MX_25G … multiple network 25 Gbit interfaces

Support for other network speeds and/or combinations of network speeds are available upon request.

2.1 Basic Usage

The syn1588® Clock_M IP core owns three basic interfaces:

- CPU interface
- Network interface
- Generated signals, imported signals

The CPU interface owns its own CPU clock signal. The network interface runs with the network clocks supplied by the external units (MAC or PHY). The generated signals are synchronous with the syn1588® clock signal. Imported signals are treated as asynchronous signal. The syn1588® Clock_M IP core takes care for the proper synchronisation of signals and data when crossing the clock domains.

When instantiating the syn1588® Clock_M IP core the CPU interface – AXI4 Lite type – shall be connected to the host CPU that runs the PTP stack (e.g. Oregano Systems' syn1588® PTP Stack). If the CPU chosen does not support AXI4 Lite interfaces a simple wrapper or bus conversion unit can be used to convert the CPU transfers to other bus protocols (e.g. Avalon_MM, AHB, etc.). The host CPU may also be attached another interface unit like PCIe.

The syn1588® Clock_M network interface(s) shall be connected to the connection of Ethernet MAC and PHY. This allows detection of Ethernet packets to be timestamped for both receive and transmit. For IEEE1588 two-step operation, this connection is purely passive; the syn1588® Clock_M does not alter the Ethernet data. The following figure shows this structure that is used for IEEE1588 two-step operation.

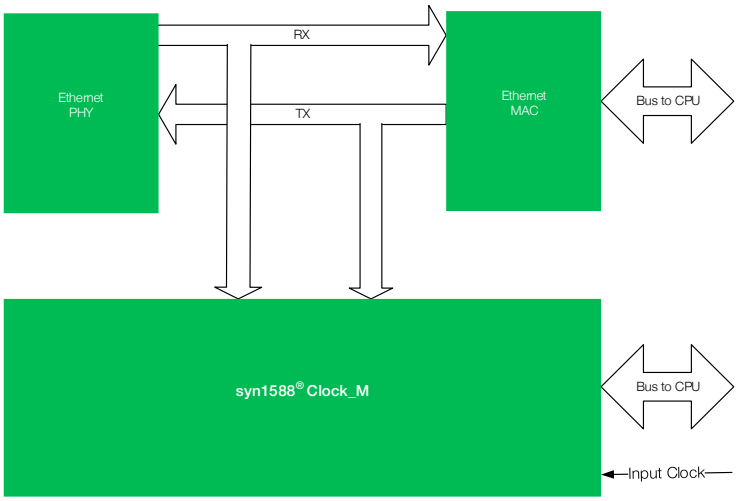

Figure 2: Attaching the syn1588® Clock_M IP core to the network for two-step operation

For IEEE1588 one-step operation, the transmit path has to be fed through the syn1588® Clock_M IP core allowing it to insert the timestamp directly into the transmit packet.

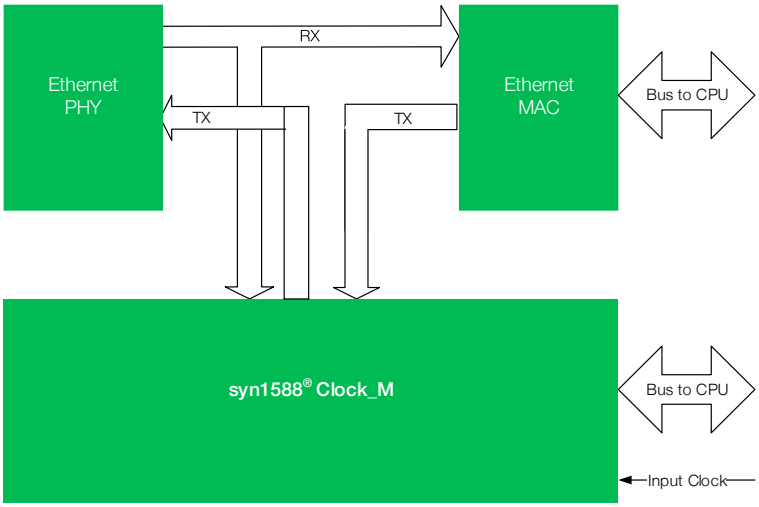

Figure 3: Attaching the syn1588® Clock_M IP core to the network for one-step operation

A typical application is the integration of the syn1588® Clock_M IP core together with the Ethernet MAC(s), the CPU and other functions in a SoC design. This allows adding high-performance IEEE1588 functions into any complex SoC system. The system might be require just the pure synchronized, accurate time or it might use generated signals like 1PPS, IRIG-B, or clocks. The CPU can be any processor ranging from a small 8 bit CISC processor like the 8051 (allowing a very small memory footprint), a 32 bit RISC softcore processor or an 64 bit hardcore processor (typically an ARM processor).

Oregano Systems providse a highly optimized syn1588® PTP Stack, which supports the complete IEEE158-2008 standard including all currently published profiles. Please contact Oregano Systems for details on the syn1588® PTP Stack. Since the load of running the syn1588® PTP Stack is not that high one does not require a dedicated processor running solely this timing service. Any existing processor might be used to run this function.

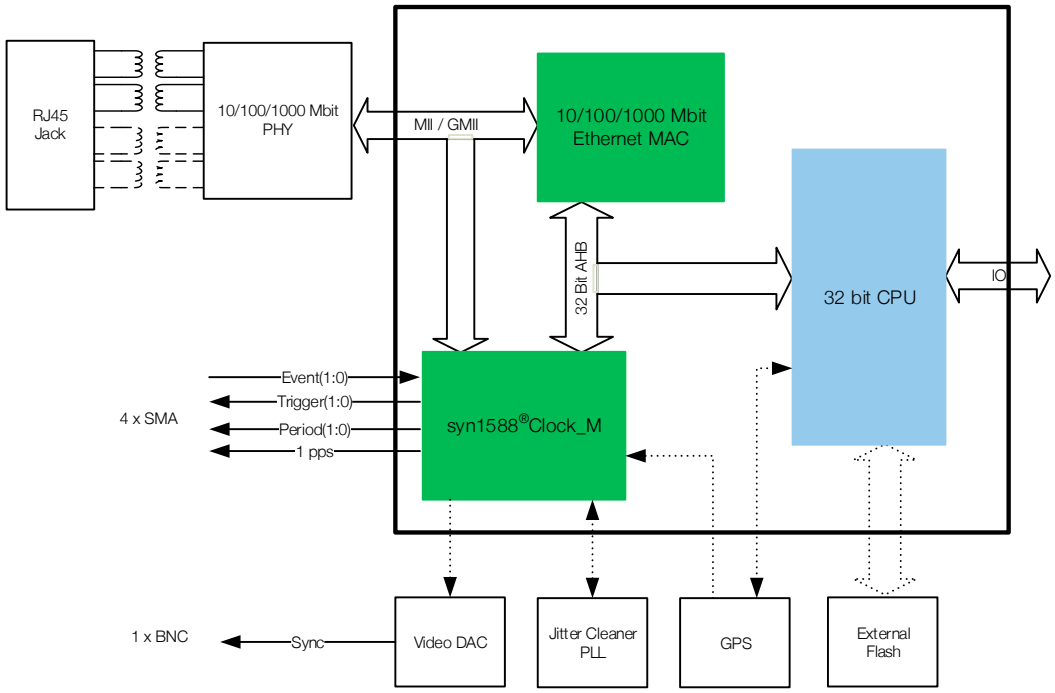

Figure 4: Example: Integrate the syn1588®Clock_M in a System on Chip Design

2.2 Functional Description

The syn1588® Clock_M IP core implements all real-time critical IEEE1588 functions enabling the control software to run on any – even simple - processor using any standard non-real-time capable operating system like Linux or Windows. The following sub-chapters briefly highlight the capabilities of the four major function blocks.

2.2.1 CPU Interface

The CPU interfaces allows reading data from and writing data to the syn1588® Clock_M IP core. The CPU interface has been designed to remove timing constraints from the control software on the host CPU. FIFOs have been used to avoid losing important data like timestamps etc. An interrupt unit can be programmed to generate interrupts for the CPU on given events.

Since the CPU interface directly interfaces to sensitive hardware and FIFO structures no burst access is supported.

2.2.2 Hardware Clock And Clock Control

This unit is the heart of the syn1588® Clock_M IP core: high-precision syn1588® hardware clock unit. There is a complex high-precision adder-based clock that implements the hardware clock.

The syn1588® hardware clock owns a resolution of 2^{-48} ns. The syn1588® hardware clock directly delivers the PTP time that may be read via the CPU interface, that is used by the timestamping units and that is made available on the IP core's interface. The sophisticated clock control unit allows set clock, rate control and rate control changes on-the-fly. The clock servo algorithm is implemented in software and controls this unit via hardware registers.

2.2.3 Network timestamping units

Whenever specific packets are sent or received on the network interface a precise timestamp has to be drawn. Each network timestamping unit is scanning a network interface. There are at least two of these network timestamping units required; one for receive and one for transmit direction. The syn1588® Clock_M IP core offers these types of network timestamping units:

- 100/1000 Mbit link speed using MII/GMII type interface
- 10 Gbit link speed using XGMII type interface
- 25 Gbit link speed using 25GMII type interface

The timestamping units are fully programmable and configurable allowing to adapt to different network protocols, VLAN, and PTP packets. Even future versions of the IEEE1588 standard – e.g. the upcoming revision 2.1 – can already be supported. All versions of the timestamping unit support both 2-step mode while1-step operation is just supported be for 100/1000 Mbit and 10 Gbit operation.

The timestamping units are capable of extract characteristic data out of the timestamped packet to allow the assignment of timestamp to the packet later on at the application layer. That's an important feature since the timestamp data and the packet data are processed in a different manner through the layers of the operating system.

2.2.4 Signal Generation

The signal generation unit generates autonomously the 1PPS signal and optionally a digital IRIG-B data stream out of the syn1588® hardware clock information. A digital IRIG-B input data stream may be read and decoded to allow synchronisation of the syn1588® hardware clock to this absolute time reference.

The signal generation unit can generate single events (named TRIGGER function) at accurate pre-programmed time. Furthermore, it can generate periodic signals like clock signals (named PERIOD function) with programmable frequency and duty cycle. The frequency of such generated accurate clocks ranges from mHz to MHz. TRIGGER functions can be used to start a PERIOD function allowing generation of precise, phase locked clock signals within a PTP network.

2.2.5 Clocking Scheme

An overview of the clock signals and clock domains used in the syn1588® Clock_M IP core is shown in the Figure 5

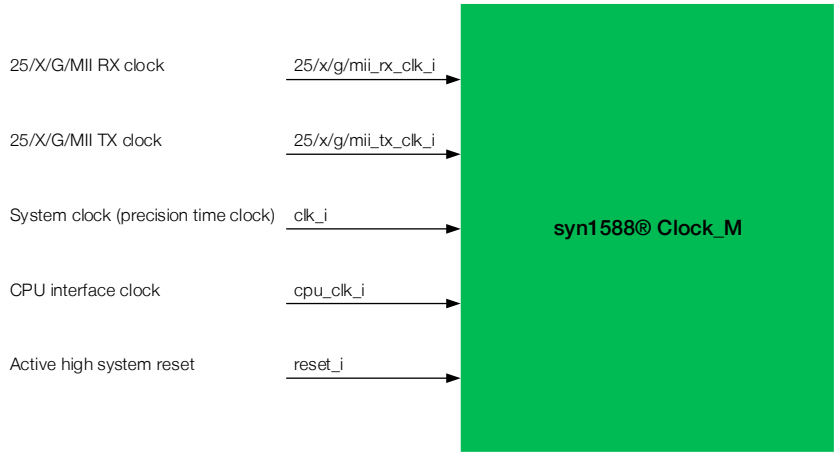

Figure 5 Clock and Reset overview at the syn1588®Clock_M IP core

2.3 Features

The syn1588® Clock_M IP core together with an Oregano Systems' syn1588® PTP Stack will synchronize its hardware clock to an IEEE1588 master or provide IEEE1588 slaves its accurate clock. The syn1588® Clock_M IP core implements all real-time functions for the IEEE1588 hardware clock and clock synchronisation. This includes timestamping of Ethernet packets sent to the network or received from the network, timestamping of external events as well as generating events at accurate points in time or accurate frequencies of arbitrary value. Thus, the syn1588® Clock_M IP core allows standard non-real-time operating systems to run the PTP applications even at high sync rates with a large number of clients without compromising the accuracy.

Special functions allow even to control the phase of any output signal throughout the whole network. Note that a PTP stack of 3rd party vendor can be used as well, however, some adaption will most likely be required.

The features of the syn1588® Clock_M IP core are summarized in the following sub-sections in detail.

2.3.1 IEEE1588 Features

- Full IEEE1588-2008 clock contained in hardware
- The clock time format is compatible to the IEEE1588 standard
- All required time critical functions are implemented in hardware. Thus, there are no real-time constraints for the software.
- Extremely fine-grained digital clock rate adjustment technique.
- Patented 1-step time stamping (on-the-fly) in transmit direction
- Generation of 1 PPS (pulse-per-second) output signal.
- Generation of digital IRIG-B output stream (DCLS mode IRIG-B000)
- Decoding of digital IRIG-B input stream (DCLS mode IRIG-B000)
- Generation of periodical signals (clocks) in a frequency range from mHZ to MHz with a resolution of 2-45 ns (PERIOD function).
- Generation of a-periodic, one-time events (TRIGGER function). TRIGGERs may be used to start the PERIOD function to allow a precise absolute phase definition in the whole PTP network
- Timestamp input signals (EVENT function). This can be used to synchronize to an external GPS-based time source via a 1 PPS signal. Minimum pulse width is 3 x syn1588® clock period.
- Events may be processed at a burst rate of 25 MHz. Sustained event rate processing capabilities are dependent on the performance of the host processor.
- All event, period, and trigger signals are strictly synchronous to the internal high accuracy clock.

2.3.2 Ethernet/Network Interface Features

- Supports 10/100 Mbit/s full duplex modes via MII
- Supports 1000 Mbit/s full duplex mode via GMII
- Supports 10 Gbit/s full duplex mode via XGMII
- Supports 25 Gbit/s full duplex mode via 25GMII
- Support for 2-step operation in all network modes
- Support for 1-step operation in 100/1000 Mbit and 10 Gbit mode
- Support for Layer 2 (raw Ethernet), IPv4, IPv6 transport protocols all with or without VLAN
- Complex programmable network scanners to detect and subsequently time stamp a configurable type of Ethernet traffic both for send and receive data
- Optional user configurable network scanners to detect and subsequently time stamp a configurable arbitrary type of Ethernet traffic both for send and receive data

2.3.3 Basic IP Core Features

- 32-bit fully compliant AXI4 Lite bus interface
- Separate CPU clock domain
- The time of the clock core is easily available via register accesses to the application software and so are the event, trigger, and period registers
- Seamless integration in SoCs
- The design of the IP core is completely synchronous for each clock with special care for clock domain crossing paths
- Coded in VHDL in a fully synchronous way
- Silicon proven
- Implementations for all major FPGA families are available

2.4 Parameterization

The syn1588® Clock_M IP Core's behaviour can be parameterized using several top level VHDL generic's. This allows the user to adapt the required FPGA/ASIC resources to be adapted to the specific needs. The following table briefly summarizes the available parameters.

Parameter	Default value	Description
g_reset_is_sync	false	If set to true synchronous reset is implemented
g_fpga_vendor	altera	FPGA vendor, selects the target technology
g_frequency	100000000	Frequency of the syn1588® clock in Hz
g_cpu_frequency	125000000	Frequency of the CPU clock in Hz
g_use_event0	true	Defines whether EVENT0 input (with FIFO) shall be implemented
g_use_event1	true	Defines whether EVENT1 input (without FIFO) shall be implemented
g_use_trigger0	true	Defines whether TRIGGER0 output (with FIFO) shall be implemented
g_use_trigger1	true	Defines whether TRIGGER1 output (without FIFO) shall be implemented
g_use_period0	true	Defines whether PERIOD0 output shall be implemented
g_use_period1	true	Defines whether PERIOD1 output shall be implemented
g_use_miits0	True	Defines whether MII timestamper 0 (default TS) shall be implemented
g_use_miits1	true	Defines whether MII timestamper 1 (user TS) shall be implemented
g_use_time2	true	Defines whether TIME2 registers shall be implemented
g_use_irigb	true	Defines whether IRIG-B I/O shall be implemented
g_use_ntp_mode	true	Defines whether NTP mode shall be implemented
g_pps_events	0	Defines the number of EVENT inputs for measurement system. (special version available upon request)
g_awidth	14	Width of the AXI4 Lite address bus

Table 1: syn1588® Clock_M IP core resource utilization for varying FPGA families.

2.5 Resource Utilization

The following table designates the resource utilization of an implementation for selected FPGA families and devices. If you need further information on resource utilization for a specific FPGA not listed, please contact Oregano Systems.

The following table shows the design resources for the syn1588® Clock_M IP core with a single 100/1000 Mbit network interface. All features have been turned on.

Technology	Type	Area
Altera/Intel Arria 10	10AS066K1F40E1SG	5531 ALM 6 M20K
Altera/Intel Cyclone V	5CEBA9F31C8	5519 ALM 6 M10K
Xilinx Kintex7	XCKU040-FFVA1156-2-E	5150 LUTs 2 RAMB36

Table 2: syn1588® Clock_M IP core resources for selected FPGA families

The following table shows the design resources for the syn1588® Clock_M IP core with a single 10 Gbit network interface. All features have been turned on.

Technology	Type	Area
Altera/Intel Stratix V	5SGSMD4K2F40C2	7797 ALM 17 M20K
Altera/Intel Arria 10	10AS066K1F40E1SG	7790 ALM 17 M20K
Xilinx Kintex7	XCKU040-FFVA1156-2-E	7069 LUTs 9 RAMB36 1 RAMB18

Table 3: syn1588® Clock_M_10G IP core resources for selected FPGA families

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2.6 Interface Signal Description

The following table summarizes all interface signals of the IP core. Please note the MII, GMII, XGMII, 25GMII interface signals are mutually exclusive.

Basic I/O Signals		
clk_i	Input	system clock (precision time clock)
cpu_clk_i	Input	AHB interface clock
reset_clk_i	Input	reset active high for syn1588® clock domain
reset_cpu_clk_i	Input	reset active high for CPU clock domain
reset_mii_txclk_i	Input	reset active high for G/MII transmit clock domain
reset_mii_rxclk_i	Input	reset active high for G/MII receive clock domain
reset_xgmii1_txclk_i	Input	reset active high for 25/XGMII transmit clock 1 domain
reset_xgmii1_rxclk_i	Input	reset active high for 25/XGMII receive clock 1 domain
syn1588® Signals		
onepps_o	Output	one pulse per second output of clock
irigb_i	Input	IRIG-B input data stream
irigb_o	Output	IRIG-B output data stream
trigger_o(1:0)	Output	two independent clock-dependent trigger outputs
event_i(1:0)	Input	two independent event inputs
period_o(1:0)	Output	two independent clock-dependent periodical output
framesync_o	Output	SMPTE frame sync signal output
framesync_i	Input	SMPTE frame sync signal input
hsync_o	Output	SMPTE horizontal sync signal output
sdi_time_27m_o(31:0)	Output	SMPTE time label data
sdi_time_90k_o(31:0)	Output	SMPTE time label data
cfcount_o	Output	SMPTE color frame counter output
cfcount_i	Output	SMPTE color frame counter input
framesync_o	Output	SMPTE sync signal
framesync_o	Output	SMPTE sync signal
syn1588time_o (95:32)	Output	IEEE1588 time
AXI4 Lite Slave Interface		
axilite_awprot_i(2:0)	Input	AXI4 Lite write address channel protection
axilite_awvalid_i	Input	AXI4 Lite write address channel valid
axilite_awready_o	Output	AXI4 Lite write address channel ready
axilite_awaddr_i(g_awidth-1:0)	Input	AXI4 Lite write address channel address
axilite_wdata_i(31:0)	Input	AXI4 Lite write data channel data
axilite_wstrb_i	Input	AXI4 Lite write data channel data strobe

axilite_wvalid_i	Input	AXI4 Lite write data channel data valid
axilite_wready_o	Output	AXI4 Lite write data channel ready
axilite_bresp_o(1:0)	Output	AXI4 Lite write response channel write response
axilite_bvalid_o	Output	AXI4 Lite write response channel valid
axilite_bready_i	Input	AXI4 Lite write response channel ready
axilite_araddr_i(g_awidth-1:0)	Input	AXI4 Lite read address channel read address
axilite_arprot_i(2:0)	Input	AXI4 Lite read address channel protection
axilite_arvalid_i	Input	AXI4 Lite read address channel valid
axilite_arready_o	Output	AXI4 Lite read address channel ready
axilite_rdata_o	Output	AXI4 Lite read response channel data
axilite_rresp_o	Output	AXI4 Lite read response channel response
axilite_rvalid_o	Output	AXI4 Lite read response channel valid
axilite_rready_i	Input	AXI4 Lite read response channel ready
Network Interface 100/1000 Mbit		
mii_txclk	Input	MII transmit clock
mii_txen_i	Input	MII transmit data valid from the Ethernet MAC
mii_txerr_i	Input	MII transmit error from the Ethernet MAC
mii_txd_from_mac(7:0)	Input	MII transmit data from the Ethernet MAC [2]
mii_txen_to_phy_o	Output	MII transmit data valid to the Ethernet PHY
mii_txerr_to_phy_o	Output	MII transmit error to the Ethernet PHY
mii_txd_to_phy_o(7:0)	Output	MII transmit data to the Ethernet PHY [2]
mii_rxclk_i	Input	MII receive clock
mii_rxdv_i	Input	MII receive data valid
mii_rxerr_i	Input	MII receive error
mii_rxd_from_phy_i(7:0)	Input	MII receive data from the Ethernet PHY [2]
XGMII Interface 10 Gbit/25 Gbit		
xgmii_txclk	Input	25/XGMII transmit clock
xgmii_txc(7:0)	Input	25/XGMII transmit control data
xgmii_txd(63:0)	Input	25/XGMII transmit data
xgmii_rxclk	Input	25/XGMII receive clock
xgmii_rxc(7:0)	Input	25/XGMII receive control data
xgmii_rxd(63:0)	Input	25/XGMII receive data

Table 4: syn1588® Clock_M family IP core: interface signals description

Notes:

[1] this signal is ignored

[2] in MII mode just the lower nibble is used

3 Detailed Specification of Functions

This section lists the main functions offered by the syn1588® Clock_M IP core.

3.1 IEEE1588 Features

3.1.1 Basic Clock Function

The syn1588®Clock_M IP core provides a hardware clock with 32 bits for counting seconds and 32 bits for counting nanoseconds. The remaining 16 most significant bits of seconds, according to IEEE1588, are handled in software.

In addition, the syn1588®clock offers 32 bit sub-nanoseconds (fractional ns) and 8 bit ultra-fractional nanoseconds to allow for extremely fine grained rate adjustment.

The current value (i.e. the TIME) of the hardware clock is readable via two 32 bit registers (32 bit nanoseconds and 32 bit seconds).

To allow a user application to access the current hardware independently from the PTP stack another pair of 32 bit registers is available enabling reading the hardware independently of the PTP stack.

The core provides a 48-bit step register. Its value defines the clock period of the syn1588®clock and added every clock cycle to the current time value; the maximum step size is 255 ns.

The clock is settable via two 32 bit registers (SHADOWTIME); again 32 bit seconds and 32 bit nanoseconds.

To speed up clock synchronization with other PTP nodes, the ADDTIME function shall allow to add the nanosecond portion of the register SHADOWTIME once (i.e. for one clock cycle) to the current TIME. This allows a single large positive increment and speeds up settling time of the filters.

While the ADDTIME function allows faster locking if the syn1588® hardware clock is behind the Grandmaster's time the STOPCLOCK function shall allow the same if the syn1588® hardware clock is in advance of the Grandmaster's time. The STOPCLOCK function shall stop incrementing (actually setting the STEP value temporarily to zero) the syn1588® hardware clock by the number of clocks given in the nanosecond portion of the register SHADOWTIME register.

An interrupt is generated upon overflow of the hardware clock TIME, if the appropriate interrupt mask bit is set.

A leap second value is stored in the register LEAP_SEC and will be applied whenever the corresponding register LEAP_APPLYTIME is matching with the time of the syn1588® clock.

Both the current leap second value and the new leap second value are accessible via register interface

3.1.2 Event Input

Two event inputs are available. The event input functions can be enabled via a bit in the EVENTCTRL register. Every rising edge of an EVENT input draws a 64 bit timestamp in the IEEE1588 format (32 bit seconds and 32 bit nanoseconds) from the hardware clock. All EVENT input 1 provide a standard register interface.

A FIFO interface is added EVENT input 0 for intermediate storage timestamps thus allowing capture of dense events without imposing real-time requirements for the software.

EVENT inputs are synchronized to the syn1588®clock using a three-stage shift register.

An interrupt is generated upon occurrence of an event, when the corresponding interrupt mask bit is set.

3.1.3 Trigger Output

By default, two programmable TRIGGER outputs are provided. The trigger functions can be enabled via a bit in the EVENTCTRL register.

A 52 bit value (20 bit seconds, 32 bit ns) defines the TIME at which the trigger is activated and will change its output state.

The following trigger events are selectable:

- set to 0
- set to 1
- toggle state

TRIGGER 1 output offers standard register interface. TRIGGER 0 output stores the requested trigger time in a FIFO, thus allowing the generation of dense trigger events without imposing real-time requirements of the software.

An interrupt is generated upon occurrence of a trigger event, when the corresponding interrupt enable bit is set

A trigger event will optionally start a selected PERIOD output.

The trigger is deactivated, if the trigger had been active (met its condition). For the trigger function with FIFO the trigger is deactivated if the FIFO is empty.

3.1.4 Period Output

Two programmable period outputs are available by default: Period 0 and Period 1. The period functions can be enabled via a bit in the EVENTCTRL register.

A 64 bit value (16 bit seconds, 32 bit ns, 16 bit fractional ns) defines the TIME at which the period changes its output state.

Upon elapse of the period timer the period output state is changed.

Upon elapse of the period timer an interrupt is generated, when the corresponding interrupt enable bit is set.

Upon elapse of the period timer the next period starts immediately, if the period timer is still enabled.

It is possible to program both a user specified initial and static period value, however, the corresponding period function has to be disabled for this operation.

An exception for Period 0 is that, it is possible to program the duty cycle for the Period 0 as well. Keep in mind that, Period 1 output is not available whenever the duty cycle function for Period 0 is enabled. Period 0/Period 1 output register pairs are used alternatively when the duty cycle function for Period 0 is enabled

It is possible to start Period 0 and Period 1 with Trigger 1 or Trigger 0

3.1.5 1 PPS Output

The 1 PPS output is enabled by default. The pulse is produced at every wrap of second of the syn1588®clock. The pulse width is configurable.

3.1.6 NTP Mode

The time stamping units can be enabled to scan for NTP event traffic by enabling the NTP mode (i.e. setting the corresponding register.

3.1.7 IRIG-B Output

An IRIG-B output (IRIG B007) is provided by default; it can be enabled via a control register bit.

3.1.8 IRIG-B Input

An IRIG-B input (IRIG B006) decoding is provided by default; it can be enabled via a control register bit.

3.2 Ethernet/Network Interface Features

3.2.1 Time Stamping Units

The syn1588® Clock_M IP core provides one timestamping unit (MII timestamper 0) on both Ethernet transmit and receive path. The second timestamping unit (MII timestamper 1) – also one unit for receive and transmit path - will act as a user configurable timestamper, when enabled.

Both MII timestamper 0 and MII timestamper 1 use a 2-step PTP timestamping function for the receive path. MII timestamper 0 provides a programmable 1-step timestamper for the transmit path. The control register TS_1STEPCTRL specifies the location of the timestamp to be inserted within the packet as well as the location of the UDP checksum to be updated.

MII timestamper 1 is limited to a programmable 2-step timestamper for the transmit path.

An interrupt will be generated when a timestamp is created or when a timestamp FIFO is full.

In addition to the general timestampers, an ultimate precision timestamper (both 1-step and 2-step) may optionally be provided for MII timestamper 0.

A pattern and mask logic shall be used by the timestampers to match specific packets.

The content of the pattern and mask is configurable based on the type of the packet that needs to be timestamped. This configuration is done via the CPU interface

A 64 bit timestamp is drawn for the packet into the respective timestamp FIFO, whenever a match with the pattern has been detected

A separate control register is available for each timestamper, thus enabling timestamping of user-specified packet types.

A timestamping FIFO control register provides information on the FIFO state.

If a packet match is detected, two sections of a maximum of 16 bytes may be extracted from the packet and stored into the timestamp FIFO as well, to allow the software to match the time stamp value with the content of the packet.

The transmit timestamp is adjusted by a PHY delay value specified in registers for 100 Mbit and 1000 Mbit to compensate structural path delay and any external PHY delay on the transmit and the receive path.

3.3 Basic IP Core Features

Each interrupt condition can be enabled via a corresponding bit in the interrupt mask register. All interrupt bits are high active. Each interrupt bit can be cleared by writing a 0 to the corresponding bit of the interrupt source register. Clearing of the interrupt bit shall be denied, if the corresponding interrupt condition is still active. The interrupt line is active as long as any enabled interrupt condition is active in the interrupt source register.

A capability register allows the detection of implemented hardware functions to ease software and driver adaptation.

4 Further Information

You are looking for further information not included in this datasheet? Please contact Oregano Systems support! We will be pleased to provide you all the required information.

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