syn1588® VIP – Revision 3

Brief Data Sheet

Version 3.3 – May 2024

Features

- Single chip PTP node
- PTP Master and Slave operation
- High precision hardware timestamping
- Clock accuracy better than 4 ns
- 1-step & 2-step PTP operation
- Patented on-the-fly timestamping
- RJ45 copper Ethernet interface
- SFP fiber interface
- 4 programmable I/O signals available via SMA jacks
  - 1 PPS output
  - Arbitrary frequency output
  - Jitter cleaner PLL for high frequency clock generation
- Video Sync Signal generation following SMPTE ST2059-1
  - Black Burst
  - Tri-Level Sync
- IRIB-B000 output
- syn1588® PTP Stack running on embedded CPU
- IEEE 1588-2008 Layer 2 & 3
- PTP support for IPv4 and IPv6
- Default, telecom, power, enterprise or broadcasting profile support
- PTP Multicast & Unicast messages
- On-board GPS receiver
- USB powered
- Serial interface via USB
- Remote firmware update
- Remote configuration of all PTP and device parameters

Options

- High stability oscillator (MEMS Super-TCXO)
- Custom software versions

syn1588® VIP Evaluation Board - Revision 3

The syn1588® VIP is a fully integrated, cost effective single chip PTP clock synchronization solution suited for a large variety of applications. Only a single external Ethernet physical layer IC is required to create a fully operational IEEE 1588-2008 node. Apart from supporting all PTP profiles published so far, it provides a number of additional features.

The syn1588® VIP is available as:

- IP Core
- Evaluation Board

The syn1588® VIP IP Core has been ported to various FPGA families of all major FPGA vendors. The IP Core is designed in a technology independent style limiting the overall porting effort.

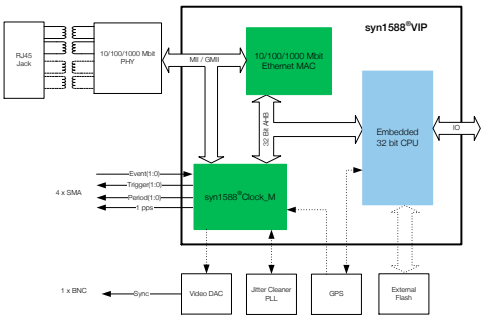
The highly efficient implementation of the PTP stack allows the syn1588® VIP to support all published PTP profiles (default, 2x broadcasting, 3x telecom, 2x power, and enterprise) with all their respective communication modes (layer 2, IPV4, and IPv6). It supports both 1-step and 2-step PTP mode.

The syn1588® VIP generates an accurate 1 PPS signal together with an arbitrary, user programmable frequency, phase locked to the local high accuracy clock. Optionally, time stamps can be generated and stored in a local buffer memory, whenever an event occurs at an external input pin.

The syn1588® VIP evaluation board is equipped with a GPS timing receiver. It will synchronize its local clock to the GPS time acting as a time traceable PTP Grand Master in the network.

In another mode of operation, the syn1588® VIP may act a GPS timing receiver without requiring an external antenna: If connected to a PTP Grand Master it will synchronize its local clock to this Grand Master. Apart from a 1 PPS signal it will generate an NMEA compatible data stream on the serial interface, effectively acting as a GPS timing receiver. Furthermore, the syn1588® VIP can generate IRIG-B compliant output data.

A syn1588® VIP reference design is freely available. Customers may receive all design data of this module enabling them to adapt it to their specific needs.



Block diagram of the syn1588® VIP – Revision 3

The syn1588® VIP evaluation board offers both an RJ45 copper and an SFP Ethernet network interface.

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Technical Specifications	
Standards	IEEE 802.3-2000 IEEE 1588-2008
Supported functions	IEEE 1588 hardware timestamping IEEE 1588 hardware clock 4 programmable IO ports GPS receiver
Operating temperature	0°C up to 50°C
Storage temperature	-40°C up to 85°C
Humidity	5% to 80% RH non-condensing

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