syn1588 ®

Application Note AN032

Determining the PHY delay of syn1588® products

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Abstract

This application describes the calculation of the PHY delay values for the syn1588® Gbit Switch and syn1588® PCIe NIC. The syn1588® Dual NIC uses the identical PHY delay values (for both network interfaces) as the syn1588® PCIe NIC – SFP version.

The receive PHY delay will be automatically subtracted from the receive timestamp while the transmit PHY delay will be added to the transmit timestamp drawn by the respective syn1588® timestamping units.

syn1588® Gbit Switch

RX PHY Delay

The timestamp is drawn following a 3-stage synchronizer engine running at 125 MHz (i.e. 8 ns) resulting in a delay of 2,5 periods (i.e. 20 ns) on the average. This value has to be subtracted from the timestamp drawn.

Additionally the Marvell PHY adds a delay that need to be subtracted from the timestamp drawn.

Description	**t [ns] GMII**	**t [ns] MII**
timestamper synchronizer stage	-20	-20
input delay 3 clocks	-24	-280
PHY delay	-191	-229
RX PHY delay register value	**-235**	**-529**

TX PHY Delay

There is one clock delay while sending the data to the PHY. This value has to be added to the timestamp drawn.

The timestamp is drawn following a 3-stage synchronizer engine running at 125 MHz (i.e. 8 ns) resulting in a delay of 2,5 periods (i.e. 20 ns) on the average. This value has to be subtracted from the timestamp drawn.

Additionally the (Marvell) PHY adds a delay that need to be added to the timestamp drawn.

Description	**t [ns] GMII**	**t [ns] MII**
output register 1 clock at port_handling	8	40
timestamper synchronizer stage	-20	-20
PHY delay	122	116
total delay	**110**	**136**

RX PHY Delay (Build 115 and newer)

The timestamp is drawn following a 3-stage synchronizer engine running at 125 MHz (i.e. 8 ns) resulting in a delay of 2,5 periods (i.e. 20 ns) on the average. This value has to be subtracted from the timestamp drawn.

Additionally the (Marvell) PHY adds a delay that need to be subtracted from the timestamp drawn.

Description	**t [ns] GMII**	**t [ns] MII**
timestamper synchronizer stage	-20	-20
input delay 1 clocks	-8	-120
PHY delay	-191	-229
RX PHY delay register value	**-219**	**-369**

TX PHY Delay (Build 115 and newer)

Starting with firmware build version 115 a modified timestamping structure is used resulting in a different delay behavior.

Description	**t [ns] GMII**	**t [ns] MII**
output delay	136	1360
timestamper synchronizer stage	-20	-20
PHY delay	122	116
total delay	**238**	**1456**

syn1588® PCIe NIC - Board Revision 1.5

RX PHY Delay

There are two input registers in the receive MAC resulting in a delay of 16 ns for GMII or 80 ns for MII. This value has to be subtracted from the timestamp drawn.

The timestamp is drawn following a 3-stage synchronizer engine running at 87,5 MHz (i.e. 11.43 ns) resulting in a delay of 2,5 periods (i.e. 28,57 ns) on the average. Two stages of the synchronizer are compensated within the syn1588® Clock_M IP core resulting in a delay of 5,72 ns. This value has to be subtracted from the timestamp drawn.

Additionally the Marvell PHY 88E1111 adds a delay that need to be subtracted from the timestamp drawn.

Description	**t [ns] GMII**	**t [ns] MII**
input registers	-16	-80
timestamper synchronizer stage	-29	-6
average compensated timestamper synchronizer delay	-6	-229
PHY device delay	-191	-315
PHY delay register value	**-213**	**-80**

PHY_DELAY register value: 0x00D50138

TX PHY Delay

There is one output register for GMII (i.e. 8 ns) in the unit topcore and one clock delay while sending the data to the PHY resulting in a delay of 16 ns for GMII or 80 ns for MII. This value has to be added to the timestamp drawn.

The timestamp is drawn following a 3-stage synchronizer engine running at 87,5 MHz (i.e. 11.43 ns) resulting in a delay of 2,5 periods (i.e. 28,57 ns) on the average. Two stages of the synchronizer are compensated within the syn1588® Clock_M IP core resulting in a delay of 5,72 ns. This value has to be subtracted from the timestamp drawn.

Additionally the Marvell PHY 88E1111 adds a delay that need to be added to the timestamp drawn.

Description	**t [ns] GMII**	**t [ns] MII**
output register & TX delay	16	80
timestamper synchronizer stage	-29	-29
average compensated timestamper synchronizer delay	-6	-6
PHY device delay	122	116
PHY delay register value	**132**	**190**

PHY_DELAY register value: 0x008400BE

syn1588® PCIe NIC - Board Revision 2.0 & 2.1

RX PHY Delay

There are two input registers in the receive MAC. This value has to be subtracted from the timestamp drawn.

The timestamp is drawn following a 3-stage synchronizer engine running at 125 MHz (i.e. 8 ns) resulting in a delay of 2,5 periods (i.e. 20 ns) on the average. Two stages of the synchronizer are compensated within the syn1588® Clock_M IP core resulting in a delay of 4 ns. This value has to be subtracted from the timestamp drawn.

Additionally the PHY (Micrel KSZ9031) adds a delay that need to be subtracted from the timestamp drawn. The PHY delay register value is the same at TSE_MAC and syn1588®Clock_M RX time-stampers.

Description	**t [ns] GMII**	**t [ns] MII**
input registers	-16	-80
average compensated timestamper synchronizer delay	-4	-4
PHY device delay	-359	-445
PHY delay register value	**-379**	**-529**

PHY_DELAY register value: 0x01780211

TX PHY Delay

There are three output register for the MAC. This value has to be added to the timestamp drawn. The 1-step timestamping logic contributes a delay of 14 clocks in GMII and 25 clocks in MII mode. In addition, there is one output register while sending the transmit data from the MAC to the syn1588®Clock_M.

The timestamp is drawn following a 3-stage synchronizer engine running at 125 MHz (i.e. 8 ns) resulting in a delay of 2,5 periods (i.e. 20 ns) on the average. Two stages of the synchronizer are compensated within the syn1588® Clock_M IP core resulting in a delay of 4 ns. This value has to be subtracted from the timestamp drawn.

Additionally, the PHY (Micrel KSZ9031) adds a delay that need to be added to the timestamp drawn.

Description	**t [ns] GMII**	**t [ns] MII**
additional output register from TX_MAC to CLOCK_M	8	40
average compensated timestamper synchronizer delay	-4	-4
1-step logic delay	112	1000
3 output register	24	120
PHY device delay	135	166
PHY delay register value CLOCK_M	**267**	**1202**
PHY delay register value TX_MAC	**275**	**1242**

PHY_DELAY register value: 0x011304DA

syn1588® PCIe NIC – SFP Version (Rev 2.1)

RX PHY Delay: Fiber Transceiver Module

The PCS/PMA unit as well as the clock crossing FIFO (9.5 clocks on the average) adds a delay that need to be subtracted from the timestamp drawn. There are two input registers in the receive MAC path; this value has to be subtracted as well.

The timestamp is drawn following a 3-stage synchronizer engine running at 125 MHz (i.e. 8 ns) resulting in a delay of 2,5 periods (i.e. 20 ns) on the average. Two stages of the synchronizer are compensated within the syn1588® Clock_M IP core resulting in a delay of 4 ns. This value has to be subtracted from the timestamp drawn.

The PHY delay register value is identical for the TSE_MAC and the syn1588®Clock_M RX time-stampers.

Description	**t [ns] GMII**
input registers	-16
average compensated timestamper synchronizer delay	-4
clock crossing FIFO	-76
PCS/PMA delay	-48
PHY delay register value	**-144**

PHY_DELAY register value: 0x00900000

TX PHY Delay: Fiber Transceiver Module

The timestamp is drawn following a 3-stage synchronizer engine running at 125 MHz (i.e. 8 ns) resulting in a delay of 2,5 periods on the average. Two stages of the synchronizer are compensated within the syn1588® Clock_M IP core resulting in a delay of 4 ns. This value has to be subtracted from the timestamp drawn.

The 1-step timestamping logic contributes a delay of 14 clocks. There is one output register while sending the transmit data from the MAC to the syn1588®Clock_M resulting in an additional delay of 8 ns respectively.

Additionally, the PCS/PMA unit as well as the clock crossing FIFO (9.5 clocks on the average) in front of the MAC add a delay that need to be added to the timestamp drawn.

Description	**t [ns] GMII**
additional output register from TX_MAC to CLOCK_M	8
average compensated timestamper synchronizer delay	-4
1-step logic delay	112
clock crossing FIFO	76
PCS/PMA delay	8
PHY delay register value CLOCK_M	**192**
PHY delay register value TX_MAC	**200**

PHY_DELAY register value: 0x00c80000

RX PHY Delay: Copper Transceiver Module

The PCS/PMA unit, the PHY in the SFP transceiver module as well as the clock crossing FIFO (9.5 clocks on the average) adds a delay that need to be subtracted from the timestamp drawn. There are two input registers in the receive MAC path; this value has to be subtracted as well.

The timestamp is drawn following a 3-stage synchronizer engine running at 125 MHz (i.e. 8 ns) resulting in a delay of 2,5 periods (i.e. 20 ns) on the average. Two stages of the synchronizer are compensated within the syn1588® Clock_M IP core resulting in a delay of 4 ns. This value has to be subtracted from the timestamp drawn.

The PHY delay register value is identical for the TSE_MAC and the syn1588®Clock_M RX time-stampers.

Description	**t [ns] GMII**	**t [ns] MII**
input registers	-16	-80
average compensated timestamper synchronizer delay	-4	-4
clock crossing FIFO	-76	-380
PCS/PMA delay	-143	-215
PHY device delay	-272	-402
PHY delay register value	**-511**	**-1081**

PHY_DELAY register value: 0x01FF0439

TX PHY Delay: Copper Transceiver Module

The timestamp is drawn following a 3-stage synchronizer engine running at 125 MHz (i.e. 8 ns) resulting in a delay of 2,5 periods on the average. Two stages of the synchronizer are compensated within the syn1588® Clock_M IP core resulting in a delay of 4 ns. This value has to be subtracted from the timestamp drawn.

The 1-step timestamping logic contributes a delay of 14 or 25 clocks respectively. There is one output register while sending the transmit data from the MAC to the syn1588®Clock_M resulting in an additional delay of 8 ns respectively.

Additionally, the PCS/PMA unit, the PHY in the SFP transceiver module as well as the clock crossing FIFO (9.5 clocks on the average) in front of the MAC add a delay that need to be added to the timestamp drawn.

Description	**t [ns] GMII**	**t [ns] MII**
additional output register from TX_MAC to CLOCK_M	8	40
average compensated timestamper synchronizer delay	-4	-4
1-step logic delay	112	1000
clock crossing FIFO	76	380
PCS/PMA delay	104	376
PHY device delay	136	280
PHY delay register value CLOCK_M	**424**	**2064**
PHY delay register value TX MAC	**432**	**2072**

PHY_DELAY register value: 0x01b00818

syn1588® PCIe NIC –Rev 2.3

RX PHY Delay: Fiber Transceiver Module

The PCS/PMA unit as well as the clock crossing FIFO (9.5 clocks on the average) adds a delay that need to be subtracted from the timestamp drawn. There are three input registers in the receive MAC path resulting in a delay of 24 ns for GMII. This value has also to be subtracted from the timestamp drawn.

The timestamp is drawn following a 3-stage synchronizer engine running at 125 MHz (i.e. 8 ns) resulting in a delay of 2,5 periods (i.e. 20 ns) on the average. Two stages of the synchronizer are compensated within the syn1588® Clock_M IP core resulting in a delay of 4 ns. This value has to be subtracted from the timestamp drawn.

The PHY delay register value is identical for the TSE_MAC and the syn1588®Clock_M RX time-stampers.

Description	**t [ns] GMII**
input registers	-24
average compensated timestamper synchronizer delay	-4
clock crossing FIFO	-76
PCS/PMA delay	-48
PHY delay register value	**-152**

PHY_DELAY register value: 0x00980000

TX PHY Delay: Fiber Transceiver Module

The timestamp is drawn following a 3-stage synchronizer engine running at 125 MHz (i.e. 8 ns) resulting in a delay of 2,5 periods on the average. Two stages of the synchronizer are compensated within the syn1588® Clock_M IP core resulting in a delay of 4 ns. This value has to be subtracted from the timestamp drawn.

The 1-step timestamping logic contributes a delay of 13 clocks or 104 ns. There is one output register while sending the transmit data from the MAC to the syn1588®Clock_M resulting in an additional delay of 8 ns respectively.

Additionally, the PCS/PMA unit as well as the clock crossing FIFO (9.5 clocks on the average) in front of the MAC add a delay that need to be added to the timestamp drawn.

Description	**t [ns] GMII**
additional output register from TX_MAC to CLOCK_M	8
average compensated timestamper synchronizer delay	-4
1-step logic delay	104
clock crossing FIFO	76
PCS/PMA delay	8
PHY delay register value CLOCK_M	**184**
PHY delay register value TX_MAC	**192**

PHY_DELAY register value: 0x00c00000

RX PHY Delay: Copper Transceiver Module

The PCS/PMA unit as well as the clock crossing FIFO (9.5 clocks on the average) adds a delay that need to be subtracted from the timestamp drawn. There are three input registers in the receive MAC path resulting in a delay of 24 ns or 120 ns respectively for GMII. This value has also to be subtracted from the timestamp drawn.

The timestamp is drawn following a 3-stage synchronizer engine running at 125 MHz (i.e. 8 ns) resulting in a delay of 2,5 periods (i.e. 20 ns) on the average. Two stages of the synchronizer are compensated within the syn1588® Clock_M IP core resulting in a delay of 4 ns. This value has to be subtracted from the timestamp drawn.

The PHY delay register value is the same at TSE_MAC and syn1588®Clock_M RX time-stampers.

Description	**t [ns] GMII**	**t [ns] MII**
input registers	-24	-120
average compensated timestamper synchronizer delay	-4	-4
clock crossing FIFO	-76	-380
PCS/PMA delay	-143	-215
PHY device delay	-272	-402
PHY delay register value	**-519**	**-1121**

PHY_DELAY register value: 0x02070461

TX PHY Delay: Copper Transceiver Module

The timestamp is drawn following a 3-stage synchronizer engine running at 125 MHz (i.e. 8 ns) resulting in a delay of 2,5 periods on the average. Two stages of the synchronizer are compensated within the syn1588® Clock_M IP core resulting in a delay of 4 ns. This value has to be subtracted from the timestamp drawn.

The 1-step timestamping logic contributes a delay of 13 clocks for GMII and 26 clocks for MII. There is one output register while sending the transmit data from the MAC to the syn1588®Clock_M resulting in an additional delay of 8 ns or 40 ns.

Additionally, the PCS/PMA unit as well as the clock crossing FIFO (9.5 clocks on the average) in front of the MAC add a delay that need to be added to the timestamp drawn.

Description	**t [ns] GMII**	**t [ns] MII**
additional output register from TX_MAC to CLOCK_M	8	40
average compensated timestamper synchronizer delay	-4	-4
1-step logic delay	104	1040
clock crossing FIFO	76	380
PCS/PMA delay	104	376
PHY device delay	136	280
PHY delay register value CLOCK_M	**416**	**2104**
PHY delay register value TX MAC	**424**	**2112**

PHY_DELAY register value: 0x01A80840

Summary

This application note described the calculation of the PHY delay correction values.

Oregano Systems
A Meinberg Company
Franzosengraben 8
A-1030 Vienna
Austria
http://oregano.at
contact@oregano.at