

syn1588[®]

Single Chip IEEE1588 Clock Synchronization Solution

syn1588[®] VIP Evaluation Board

Board Revision 3 - Data Sheet

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0 Legals

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1 Overview

The syn1588[®] VIP Evaluation Board enables a cost effective, highly integrated, single chip IEEE1588 based clock synchronization solution. Only a single external Ethernet PHY is required to create a fully functional IEEE1588 node supporting either the default or the telecom profile

The entire clock synchronization algorithms are computed in an on-chip 32 bit RISC processor which runs the complete syn1588[®] PTP Stack together with a light-weight IP stack. The syn1588[®] VIP design offers a standard 10/100/1000 Mbit/s Ethernet network interface with enhancements to provide the system with accurate clock synchronization via Ethernet following the IEEE1588-2008 standard.

Starting with Revision 3 of the syn1588[®] VIP Evaluation Board there are two types of network interfaces available, which can be selected by the user using a switch:

- Standard RJ45 copper interface
- SFP type fibre interface

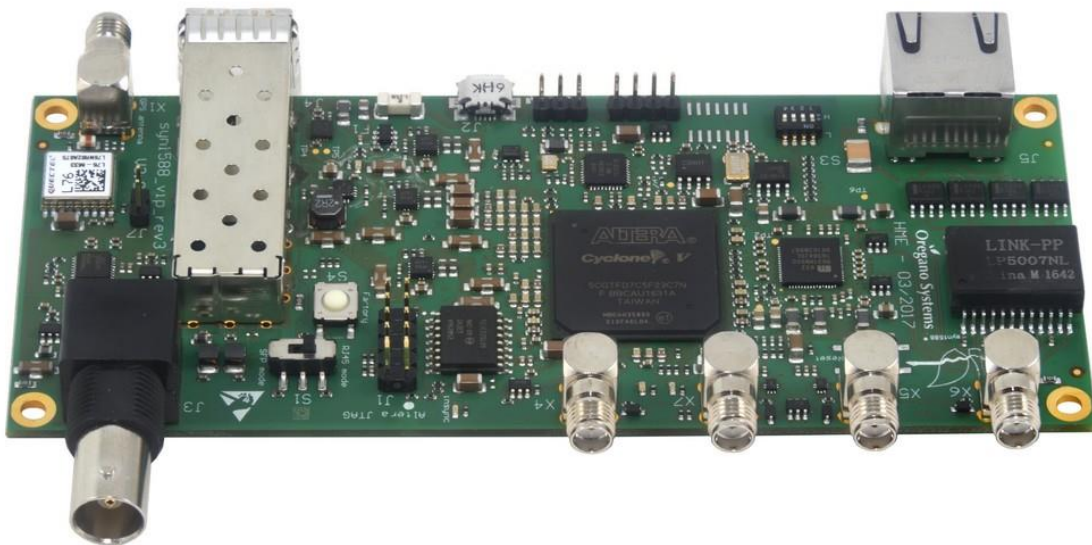


Figure 1 syn1588[®] VIP Evaluation Board – Revision 3: front view

Changing the switch state is just allowed in the power-off state of the syn1588[®] VIP Evaluation Board.

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The syn1588[®] VIP Evaluation Board delivers a 1PPS output signal as well as a user programmable, synchronized frequency. A NMEA-compatible stream may be generated on the serial interface. An IRIG-B compatible output and input is available as well. The syn1588[®] VIP Evaluation Board can generate high-accuracy clock signals, events and - starting with revision 3 - Video sync signals.

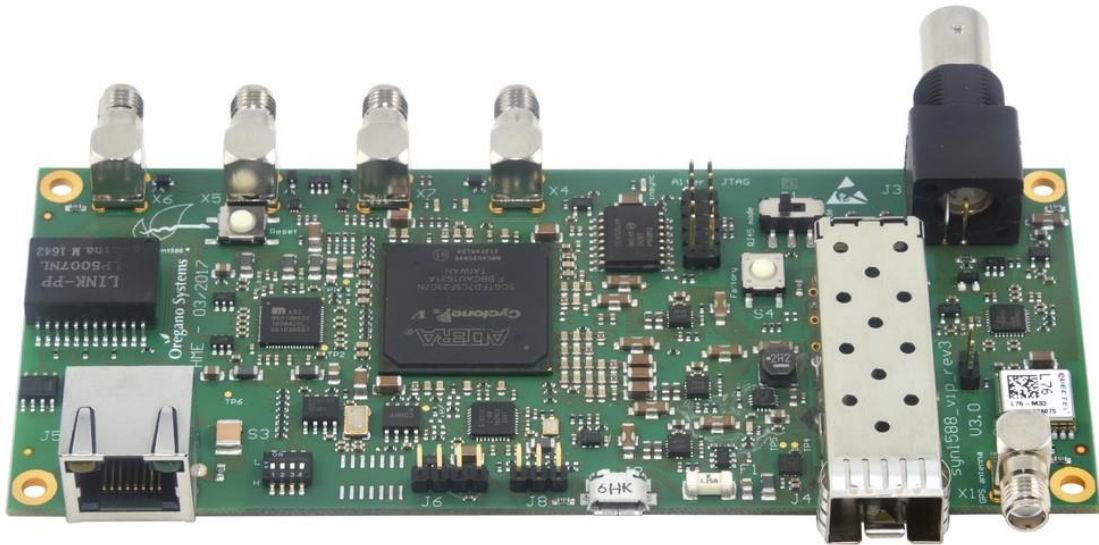


Figure 2 syn1588[®] VIP Evaluation Board – Revision 3: rear view

This latest board revision is USB powered (USB 3.0) and offers a small on-board GPS receiver as well. The operation of the syn1588[®] VIP Evaluation Board is controlled remotely via IEEE1588 management messages. Both, a command line tool (ptpmmm) as well as a graphical user interface (ptpmmm GUI) are available for managing IEEE1588 nodes remotely.

1.1 Block Diagram

Figure 1 shows the block diagram of the syn1588[®] VIP Evaluation Board (board revision 3).

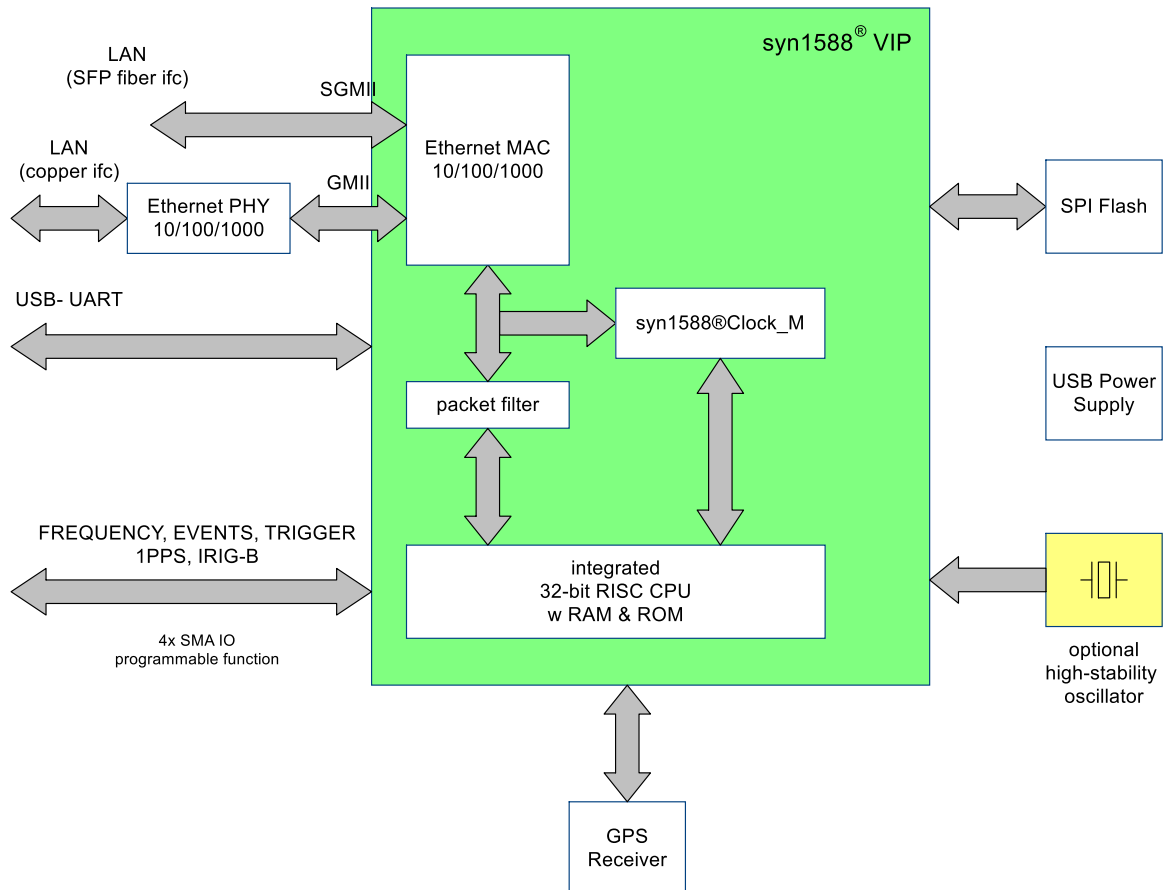


Figure 3 syn1588[®] VIP Evaluation Board – Revision 3: system diagram

The syn1588[®] VIP Evaluation Board is sophisticated, cost-effective single-chip IEEE1588 solutions. It merely requires an external Ethernet PHY. A SPI flash is used to store the device's configuration as well as the user defined parameters.

1.2 Ordering Information

The syn1588[®] VIP Evaluation Board can directly be ordered at Oregano Systems and at our distributors (see our web site <http://oregano.at> for details).

1.2.1 Ordering Codes

syn1588[®] VIP Evaluation Board: syn1588 VIP-evalbrd

2 Features

- Fully IEEE1588-2008 standard compliant network node in a single chip
 - IEEE1588-2008 two-step clock operation
 - Optionally IEEE1588-2008 one-step clock operation
- syn1588[®] PTP stack binary included (running on integrated 32 bit CPU core)
- Single chip solution (except the external Ethernet PHY)
 - No external memory devices required
- Support for 100/1000 Mbit/s operation (MII and GMII mode) following IEEE802.3-2005 standard
- Four programmable user IOs for 1PPS, EVENT, TRIGGER, PERIOD, IRIG-B
- 1PPS output signal (one pulse per second)
- IRIG-B data stream input and output (IRIG-B007, DCLS signal, no carrier, BCD + BCD_Year)
- Frequency output with a selectable frequency in the range from 1 MHz to 156 MHz
 - Frequency is user selectable
 - Optionally using external jitter cleaner PLL
 - Other fixed frequencies (eg. 10 MHz or 25 MHz) can be provided upon request
- UART may output time information in GPS compatible NMEA format
 - Suited for GPS replacement via LAN
- On-board GPS receiver
 - May be used to deliver absolute time for master mode
 - Supports active GPS antenna (3V3 feed)
- On-board jitter cleaner PLL for generating accurate, synchronized single-ended frequencies up to 156.25 MHz
- On-board video sync generation logic

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- Network layer 2 (raw Ethernet) or network layer 3 (Internet Protocol) operation supported via firmware options
- PTP management interface is supported ([IEEE 1588-2008] Clause 15) allowing remote management
- Configuration of the syn1588[®] VIP node may be stored onto the on-board SPI Flash memory
- Dual boot capability
 - factory default firmware
 - user firmware
 - Revert to factory default mechanism available
- Remote update of user firmware
- Clock accuracy better than 20 ns

3 Functional Description

The syn1588[®] VIP Evaluation Board is entirely self-contained and does not need any user interaction to operate. There is only one switch S1, which selects the network interface.

Via the PTP management interface status information can be gathered in layer 3 mode and clock parameters as well as I/O options can be configured.

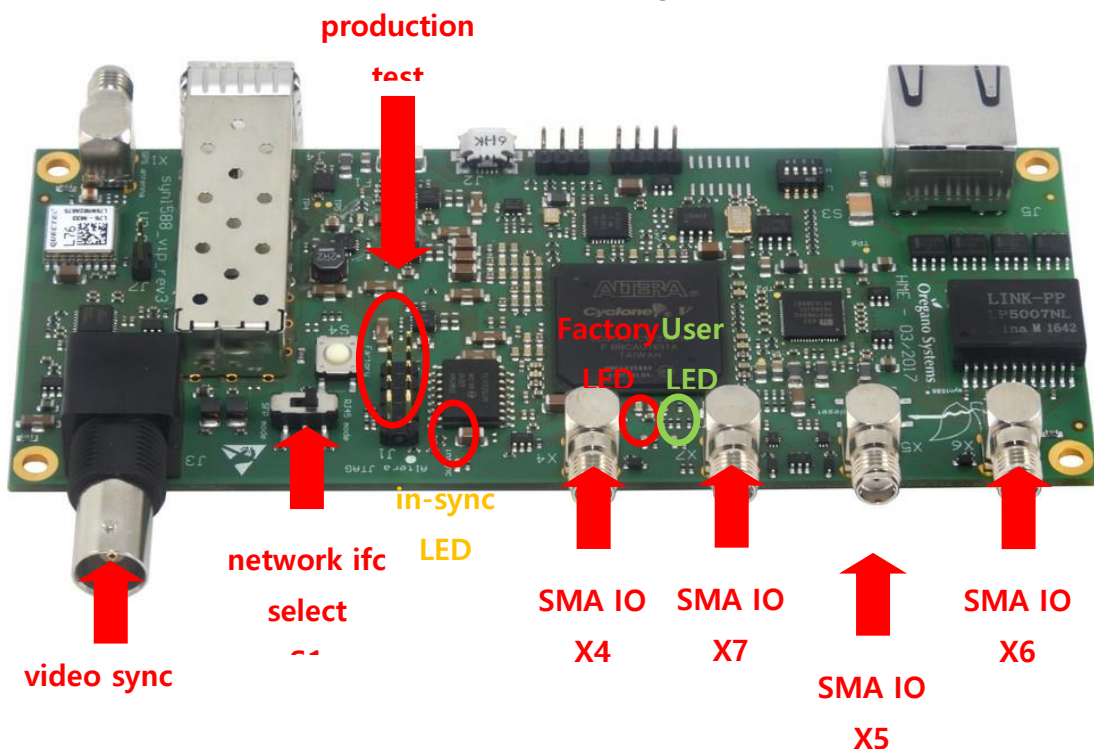


Figure 4 syn1588® VIP Evaluation Board – Revision 3: front side connectors

Oregano Systems' syn1588® VIP Evaluation Board is a highly integrated embedded IEEE1588 node. It's rich feature set allows to use the unit as a sophisticated autonomous PTP slave in the network as well as a simple, reliable PTP Grandmaster. All functions can be remotely monitored or controlled via the network.

Oregano Systems' syn1588® VIP Evaluation Board is a fully functional reference board for the syn1588® VIP IP core. Customers may receive all design data of this reference board enabling them to easily adapt this design to their specific needs.

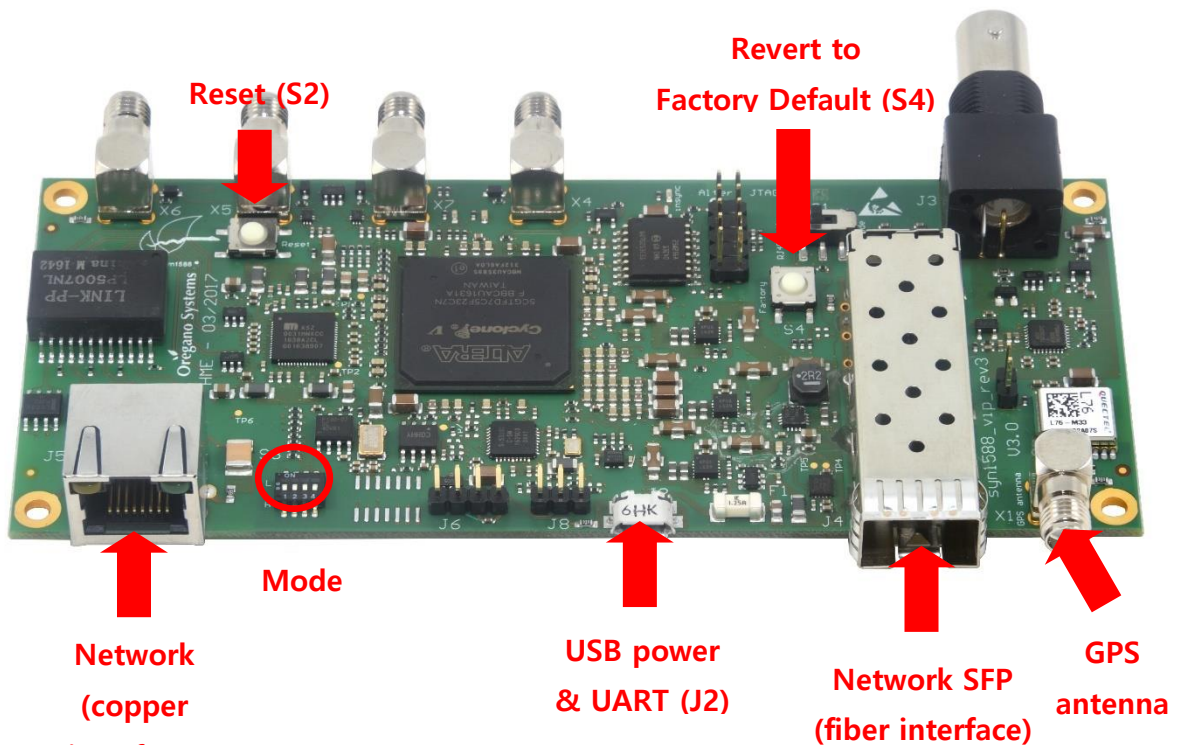


Figure 5 syn1588® VIP Evaluation Board – Revision 3: rear side connectors

3.1 Network Interface Selector (S1)

Using the network interface selector switch S1 one can choose which network interface shall be used: the standard copper RJ45 connector or the SFP fibre interface. Changing the network interface selector switch' state is just allowed in the power-off state of the syn1588[®] VIP Evaluation Board. Unexpected behaviour of the unit might occur, when the switched is activated during normal operation of the board.

Please note that the selected network interface will become active with the next power-on sequence. Please further note that both network interfaces cannot be active at the same time.

3.2 USB Power and Serial Logging

The USB interface connector J2 acts as both power supply and serial interface for logging purposes.

3.3 SMA I/O X4 to X7

The four SMA connectors may be assigned a specific input or output function. There is a register IOMATRIX that specifies the usage of these four SMA connectors. This register can be remotely set (preset) via the PTP management interface.

| Bits | Description |
|-----------------|--|
| IOMATRIX(31-28) | Source definition for IRIG-B input unit (range 0-4: SMA connectors only) |
| IOMATRIX(27) | Level definition for SMA connector 3 input (NIC-X5/ VIP-nc) 0 = high active 1 = low active (inverted internally) |
| IOMATRIX(26) | Level definition for SMA connector 2 input (NIC-X6/ VIP-X4) 0 = high active 1 = low active (inverted internally) |
| IOMATRIX(25) | Level definition for SMA connector 1 input (NIC-X7/ VIP-X5) 0 = high active 1 = low active (inverted internally) |
| IOMATRIX(24) | Level definition for SMA connector 0 input (NIC-X4/ VIP-X6) 0 = high active 1 = low active (inverted internally) |
| IOMATRIX(23:20) | Source definition for event 1 input of syn1588® Clock_M |
| IOMATRIX(19:16) | Source definition for event 0 input of syn1588® Clock_M |
| IOMATRIX(15:12) | Source definition for SMA connector X5 |
| IOMATRIX(11:8) | Source definition for SMA connector X6 |
| IOMATRIX(7:4) | Source definition for SMA connector X7 |
| IOMATRIX(3:0) | Source definition for SMA connector X4 |

Table 1: IOMATRIX register: description

| Value | Output to SMA connector | Source of the EVENT inputs, Source of IRIG-B decoder (0 to 4 only) |
|-------|--|---|
| 0x0 | disabled (output tri-state, used as input) | '0' |
| 0x1 | SMA connector X4 | SMA connector X4 |
| 0x2 | SMA connector X5 | SMA connector X5 |

| Value | Output to SMA connector | Source of the EVENT inputs, Source of IRIG-B decoder (0 to 4 only) |
|-------|--|---|
| 0x3 | SMA connector X6 | SMA connector X6 |
| 0x4 | SMA connector X7 | SMA connector X7 |
| 0x5 | period0_o signal of syn1588 [®] Clock_M | period0_o signal of syn1588 [®] Clock_M |
| 0x6 | period1_o signal of syn1588 [®] Clock_M | period1_o signal of syn1588 [®] Clock_M |
| 0x7 | trigger0_o signal of syn1588 [®] Clock_M | trigger0_o signal of syn1588 [®] Clock_M |
| 0x8 | trigger1_o signal of syn1588 [®] Clock_M | trigger1_o signal of syn1588 [®] Clock_M |
| 0x9 | 1pps_o signal of syn1588 [®] Clock_M | 1pps_o signal of syn1588 [®] Clock_M |
| 0xa | IRIG-B signal of syn1588 [®] Clock_M | '0' |
| 0xb | RX timestamp strobe (for debugging) | decoded 1PPS signal from IRIG-B input unit |
| 0xc | TX timestamp strobe (for debugging) | '0' |
| 0xd | filtered period1_o via external jitter cleaner PLL | '0' |
| 0xe | 1pps input from GPS | 1pps input from GPS |
| 0xf | Framesync output | '0' |

Table 2: Encoding of sources for IOMATRIX register

3.4 In-Sync LED

Depending on the current PTP mode of the device, the In-Sync LED (yellow) signals the nodes current synchronization state. Please see Table 3 for details. The LED is inactive after start-up.

| PTP State | In-Sync LED |
|-----------|--|
| Master | The In-Sync LED is active when the IEEE1588 node is synchronized to an external source (e.g., a GPS receiver), otherwise inactive. |
| Slave | As soon as the IEEE1588 node is synchronized to its master the In- |

| PTP State | In-Sync LED |
|-----------|---|
| | Sync LED is active, otherwise inactive. |

Table 3: In-Sync LED interpretation

3.5 GPS Receiver

The syn1588[®] VIP Evaluation Board Revision 3 offers an on-board GPS receiver. This allows in master mode an external absolute time reference without any external components. One just has to plug-in the GPS antenna and configure the syn1588[®] VIP to use the GPS signals as the reference.

In order to enable GPS master mode, one has to use the syn1588[®] PTP Management Tool. The following commands have to be issued to the syn1588[®] VIP Evaluation Board Revision 3 in order to enable the internal GPS receiver:

```
param 8CA5A1FFFE00051A 1 0 esync 0x2
clkman 8CA5A1FFFE00051A 1 0 0x200 0x00e300e9
save 8CA5A1FFFE00051A 1 0
```

The “param esync” command sets the synchronization mode of the syn1588[®] VIP’s sync engine to 0x2 which means GPS synchronization. The “clkman” command routes the 1PPS signal from the GPS receiver to the event input of the syn1588[®] VIP Evaluation Board sync engine. The “save” command saves the performed modification to flash so the settings are reloaded after a power-cycle of the syn1588[®] VIP.

Please refer to chapter 8 of the syn1588[®] User Guide for further details about the syn1588[®] PTP Management Tool and how to use it.

3.6 Accuracy

The overall accuracy within an IEEE1588 network or in other words the maximum deviation between the 1 PPS clock signals of any two given nodes is both dependent on several different configuration parameters and on the hardware of the nodes itself.

The latter has two major aspects to consider: On the one side, the resolution of the high accuracy IEEE1588 clock located at the network interface defines the resolution of the time

stamps gathered will scanning for IEEE1588 timing related packets. Furthermore, the stability of the oscillator driving the high accuracy clock is of equal importance when evaluating accuracy. With respect to configuration parameters the rate of the sync and, to a certain extent, the rate of the delay request packets have considerable impact on the overall accuracy. For more details please refer to the white paper on highly accurate clock synchronization authored by Oregon Systems.

The local clock of the syn1588® VIP Evaluation Board Revision 3 offers a resolution of less than 4 ns. If it is equipped with a 4 ppm 25 MHz oscillator (TCXO). Thus, an accuracy in the range of ± 30 ns can be achieved if the message rate is selected in the range on 1 sec.

3.7 FPGA Configuration LEDs

There are two LEDs that flag which configuration is currently been used:

- D13, red LED, factory default configuration
- D12, green LED, user configuration

Both LEDs are located between the SMA connectors X4 and X7 (see Figure 4).

3.8 Reset Button (S2)

The reset push button S2 allows to reset both the hardware as well as the software (CPU) of the syn1588® VIP Evaluation Board Revision 3 to bring the unit back into a well-known initial state.

3.9 Revert to Factory Default Button (S4)

If the syn1588® VIP Evaluation Board Revision 3

- had been misconfigured
- or one does not remember the actual network configuration of the unit
- or one would like to switch to a well-known firmware version

simply press the Revert-to-Factory-Default-Button S4 (see Figure 5) until the red configuration LED D13 is permanently on. This flags that the factory default configuration is active which does not load the stored parameters from the SPI flash device; well-

known default parameters are now used enabling the user to properly re-configure the whole parameter set.

3.10 Remote Configuration

The syn1588[®] VIP may be configured using IEEE1588 Management Messages received via the Ethernet interface. Thus, the syn1588[®] VIP unit can be fully remotely configured. The syn1588[®] VIP management interface is fully compliant to the IEEE1588 standard. Three vendor specific commands have been implemented to read/write from/to syn1588[®] VIP units (param, update, clkman).

The Oregano Systems' syn1588[®] PTP Management Tool "ptpmmm" is the tool of choice for configuring syn1588[®] VIP nodes. This tool can send IEEE1588 standard management messages as well as the Oregano specific IEEE1588 management messages. Please contact Oregano Systems support to receive a copy of the syn1588[®] PTP Management Tool free of charge (either via the web site <http://oregano.at> or via email contact@oregano.at).

Note, that the factory default configuration uses default parameters while the user configuration loads the previously stored parameters from the non-volatile configuration memory during start-up.

3.10.1 Example 1: Identifying syn1588® VIP Nodes

The basic usage of the ptpmmm tool in combination with the syn1588® VIP is to read the value of a syn1588® Clock register. This is accomplished in the following way. First invoke the ptpmmm utility on any node in your network that is connected to your syn1588®VIP unit (the unit has to be visible in terms of IP/UDP traffic).

```
# ./ptpmmm
syn1588(R) PTP Management Tool - IEEE1588-2008
Build date: Jul 25 2017 - V 1.4-167 Rev g2975a1f
Copyright (c) Oregano Systems - Design & Consulting GesmbH 2005-2017
Confidential unpublished data - All rights reserved

Command line: ptpmmm
>
```

After invocation of ptpmmm one can enter commands that send IEEE1588 management messages to the syn1588® VIP nodes in the network. Note that PTPMMM has no command prompt or the like to facilitate batch operation and automated post processing of output data.

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To discover all syn1588® VIP nodes in the network issue the “clock” command. You do this by typing “clock” followed by Enter. This should give a similar output like this:

```
# ./ptpmmm
syn1588(R) PTP Management Tool - IEEE1588-2008
Build date: Jul 25 2017 - V 1.4-167 Rev g2975alf
Copyright (c) Oregon Systems - Design & Consulting GesmbH 2005-2017
Confidential unpublished data - All rights reserved

Command line: ptpmmm
>clock
001EC0FFFE85B2AF 1 OC "IEEE 802.3" 001EC085B2AF IPv4:0A000271 FFFFFFF "Oregon Sy
stems; syn1588(R) PCIe NIC; 00:1E:C0:85:B2:AF" "HW build 779; syn1588(R) Clock M
2.3.2; SW 1.4-37 Rev ge6e6d95" "syn1588_NIC" 001B19000100
0004A3FFFE2D4627 1 OC "IEEE 802.3" 0004A32D4627 IPv4:0A004627 FFFFFFF "Oregon Sy
stems; syn1588(R) PCIe NIC; 00:04:A3:2D:46:27" "HW build 757; syn1588(R) Clock M
2.3.1; SW 1.4-51 Rev gfc70f1e" "syn1588_NIC" 001B19000100
8CA5A1FFFE00054E 1 OC "IEEE 802.3" 8CA5A100054E IPv4:0A00028B FFFFFFF "Oregon Sy
stems; syn1588(R) VIP; 8C:A5:A1:00:05:4E" "HW build 686; syn1588(R) Clock M 2.3.
2; SW 1.4-42 Rev g71fcd42-dirty" "syn1588_VIP_Rev3.0" 001B19000100
0050C2FFFE2DFAE 1 ? "IEEE 802.3" 0050C2C2DFAE IPv4:0A000102 000F0C "MBG;;" ";;"
";" 001B19000100
0004A3FFFF4B400A 1 ? "IEEE 802.3" 0004A34B400A IPv4:0A0002D8 FFFFFFF "Oregon Sys
tems; syn1588(R) VIP; 00:04:A3:4B:40:0A" "HW build 551; syn1588(R) Clock M 2.3.0
; SW 1.2.238" "syn1588_VIP_Rev2.1" 001B19000100
>
```

3.10.2 Example 2: Reading syn1588[®] VIP Registers

The syn1588[®] VIP supports a proprietary extension to the PTP management interface. This extension is made up of only one - very powerful – command: “clkman”. It allows to read and write to the hardware registers of the syn1588[®] VIP.

For example, with this command one can read the version of the syn1588[®] Clock IP core that is embedded in the node. The version of the clock is located in register 0x0. So to get the version of the clock one issues a “clkman” command to read clock register 0x0.

```
# ./ptpmmm
syn1588(R) PTP Management Tool - IEEE1588-2008
Build date: Jul 25 2017 - V 1.4-167 Rev g2975a1f
Copyright (c) Oregano Systems - Design & Consulting GesmbH 2005-2017
Confidential unpublished data - All rights reserved

Command line: ptpmmm
> clock
8CA5A1FFFE00054E 1 OC "IEEE 802.3" 8CA5A100054E IPv4:0A00028B FFFFFFF "Oregano Systems; syn1588(R) VIP; 8C:A5:A1:00:05:4E" "HW build 686; syn1588(R) Clock M 2.3.2; SW 1.4-42 Rev g71fcd42-dirty" "syn1588_VIP_Rev3.0" 001B19000100
>clkman 8CA5A1FFFE00054E 1 0 0x0
8CA5A1FFFE00054E 1 0x4D323332
>
```

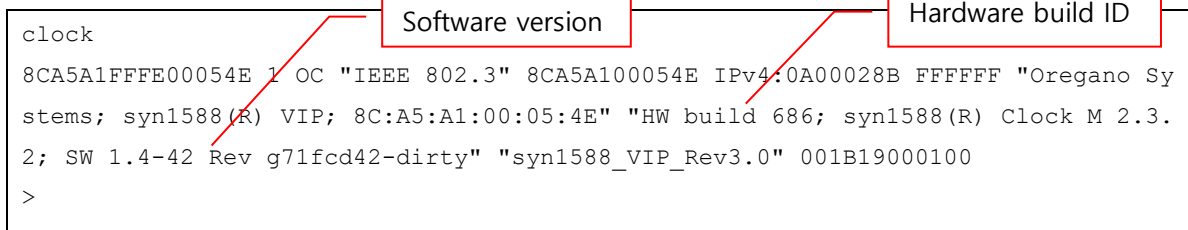
The result of the “clkman” command is always displayed in hexadecimal notation. Since the clock version is encoded as four ASCII characters the result of 0x4d323332 has to be converted in ASCII to get the clock version: 0x4d equals ‘M’, 0x32 equals ‘2’, 0x33 equals ‘3’, and finally 0x32 equals ‘2’. So the clock version is ‘M232’.

3.10.3 Setting and Storing Parameters

The syn1588® VIP Evaluation Board Revision 3 supports managing (read/get and write/set) and non-volatile storage of its parameters. The parameters are stored in the external SPI flash memory by using the management command "save".

One uses the IEEE1588 management command CLOCK to determine the software revision.

```
clock
8CA5A1FFFE00054E 1 OC "IEEE 802.3" 8CA5A100054E IPv4:0A00028B FFFFFF "Oregano Sy
stems; syn1588(R) VIP; 8C:A5:A1:00:05:4E" "HW build 686; syn1588(R) Clock M 2.3.
2; SW 1.4-42 Rev g71fcd42-dirty" "syn1588_VIP_Rev3.0" 001B19000100
>
```



There are the following group of parameters that may be modified and stored:

- network configuration
- hardware parameters
- syn1588® PTP Stack options
- clock servo parameters

The following sub chapters describe each set of parameters as well as the command used to read (get) and write (set) the parameters.

3.10.3.1 Network Parameters

syn1588® VIP network configuration is read and written using the Oregano Systems' specific IEEE1588 management command "param".

| Name | Brief Description | Effective | Default Value |
|----------|--|-----------|---------------|
| dhcp | Enable/Disable DHCP | Reboot | 1 |
| ipaddr | Use the following IP if DHCP is disabled | Reboot | 10.0.0.20 |
| subnet | Use this sub net mask if DHCP is disabled | Reboot | 255.0.0.0 |
| gateway | Use this gateway if DHCP is disabled | Reboot | 10.0.0.1 |
| nwmode* | Specifies if multicast, unicast or both is used M ... multicast U ... unicast B ... both | Reboot | M |
| nwproto* | Selects the network protocol: layer2 ... Using PTP over IEEE802.3 IPv4 ... Using PTP over IPv4/UDP | Reboot | IPv4 |
| vlan* | Enable (1) or disable (0) the VLAN function | Reboot | 0x0 |
| vlanid* | Set the VLAN Id (range 0 .. 4095) | Reboot | 0x0 |
| dfs | Set the Differentiated Services Field of the IPv4 header (0x0..0xFF) | Reboot | 0x0 |
| grantor0 | IP address of unicast master 0 (if available) | Reboot | N/A |
| grantor1 | IP address of unicast master 1 (if available) | Reboot | N/A |

Table 4 List of network parameters

Note *: Due to the memory limitations of the embedded 1588 solution every firmware version of the syn1588®VIP implements a well-defined subset of PTP profiles and thus network modes. Thus, these parameters might not be editable at all. Changing the PTP profile might require another syn1588®VIP firmware version which is in fact no limitation at all.

By default, DHCP and multicast mode are enabled. Please make sure that the "save" command has been executed and the device is rebooted (power off/on or "init" management command) after setting a network parameter. If unicast is enabled, the grantor0 and grantor1 parameter offer the possibility to configure two different unicast masters. They are specified by using their IPv4 address. To delete a grantor, the IP address 0.0.0.0 is used. By sending this address, the grantor is deactivated.

Example

First read the IP address and set the IP address to 10.0.0.3 in a second step.

```
param 8CA5A1FFFE00054E 1 0 ipadr
8CA5A1FFFE00054E 1 255.255.255.255
> param 8CA5A1FFFE00054E 1 0 ipadr 10.0.0.3
8CA5A1FFFE00054E 1 DONE
> save 8CA5A1FFFE00054E 1 0
8CA5A1FFFE00054E 1 DONE
>
```

3.10.3.2 syn1588® PTP Stack Parameters

The following parameters are standard IEEE1588 parameters where dedicated IEEE1588 management messages are available. Therefore, they are not configured with the "param" command. The fourth column "Command" in Table 5 shows the respective management message and thus ptpmmm command required for set/get this parameter.

| Name | Brief Description | Effective | Command | Default Value |
|-------------------------|--|-----------|----------|---------------|
| Accuracy | set clock accuracy (range 0..255) | instantly | accuracy | 39 |
| Announce Interval | set announce interval (log2 range -4..4) | instantly | aival | 1 |
| Delay Mechanism | delay mechanism used: E .. end-to-end (0x01) P .. peer-to-peer (0x02) 0 .. no delay mechanism at all (0xFE) | instantly | dlymech | 0x01 |
| Domain | set Domain (range 0..255) | instantly | domain | 0 |
| pDelay Request Interval | set minimum path delay request interval (log2 range 0..5) | instantly | pival | 0 |
| Priority 1 | sets Priority1 (range 0..255) | instantly | prio1 | 128 |
| Sync Interval | set synchronization interval (log2 range -8..+8) | instantly | sival | 0 |
| User | Assigns a user description to the clock | instantly | user | syn1588_nios |

Table 5 List of IEEE1588 standard parameters

Example

Read the delay mechanism used; set the delay mechanism to peer-to-peer (0x2).

```
dlymech 8CA5A1FFFE00054E 1 0
8CA5A1FFFE00054E 1 E
> dlymech 8CA5A1FFFE00054E 1 0 0x2
8CA5A1FFFE00054E 1 DONE
>
```

3.10.3.3 Extended syn1588® PTP Stack Parameters

The extended parameters of the syn1588® PTP stack are read and written using the Oregon Systems' specific IEEE1588 management command "param". Table 16 shows all available parameters.

Example

Read the current log level of the selected clock; set the log level to verbose mode (0x2).

```
param 8CA5A1FFFE00054E 1 0 loglevel
8CA5A1FFFE00054E 1 0x1
>param 8CA5A1FFFE00054E 1 0 loglevel 0x2
8CA5A1FFFE00054E 1 DONE
>
```

| Name | Brief Description | Effective | Default Value |
|------------|---|-----------|---------------|
| adjival | Sets the clock adjust interval (log2 range 0..8) | instantly | 0 |
| twostep | Use 2-step (1) or 1-step (0) mechanism | instantly | 1 |
| dlyreqival | Sets the minimum delay request interval offset added to syncInt (log2 range 0..8) | instantly | 4 |
| variance | set clock variance (range 0..0xFFFF) | instantly | 0xFFFF |
| class | set clock class [248] M_EXT...Master on External Reference (6) M_HOLD...Master on External Reference (in Holdover) (7) M_NSUNC..Master on External Reference (not synchronized) (52) M_SLAVE..Master on External Reference (may be Slave) (187) S...Slave Only (default 255) | instantly | 255 |
| dlyasym | delay asymmetry correction in scaled nanoseconds | instantly | 0 |

| Name | Brief Description | Effective | Default Value |
|--------------------|--|-----------|---------------|
| boundary | Sets a boundary for offset to master in scaled nanoseconds | instantly | 0 |
| loglevel | change verbosity level (range 0..4) [default 0] (if available) | instantly | 4 |
| vsync ¹ | Change vSync parameters (range 32 bit signed) [default 0] | instantly | 0 |

Table 6 List of extended syn1588[®] PTP Stack parameters

Note 1: The vsync parameter for the param command is supported for syn1588[®]VIP Revision 3. Three parameters are encoded to a single 32 bit signed word. Three values are combined to this single 32 bit word. The least significant byte denotes the video mode (default = 0 .. 525i). Bit 8 is set if the video DAC shall be used for generating the video sync signal. The upper 16 bit denote the offset in ns (signed 16 bit) of the video sync signal with respect to the master.

3.11 Remote Initialisation

The syn1588[®] VIP may be remotely initialized using IEEE1588 Management Messages. Again ptpmmm utility is used for sending the commands. The INIT command (standard IEEE1588 INITIALIZE management messages) is used for this purpose. The parameter of the INIT command defines the type of the initialization that shall be performed.

| Command | Parameter | Description |
|---------|-----------|--|
| init | 0x0 | CPU software reset |
| init | 0x8000 | hardware re-configuration |
| init | 0x8001 | syn1588 [®] PTP Stack re-initialization |

Table 7 INIT command parameter description

The following examples shows how to request a CPU software reset of a syn1588[®] VIP clock.

```
# ./ptpmmm
syn1588(R) PTP Management Tool - IEEE1588-2008
Build date: Jul 25 2017 - V 1.4-167 Rev g2975a1f
Copyright (c) Oregano Systems - Design & Consulting GesmbH 2005-2017
Confidential unpublished data - All rights reserved

Command line: ptpmmm
>
> init 8CA5A1FFFE00054E 1 0 0x0
8CA5A1FFFE00054E 1 DONE
>
```

3.12 Remote Firmware Update

The syn1588® VIP Evaluation Board Revision 3 supports two configurations in its non-volatile configuration device:

- The factory default configuration
- The user configuration

The factory default configuration is programmed onto the syn1588® VIP Evaluation Board Revision 3 during the production test and cannot be altered by the user. The user configuration can be updated using the remote firmware update procedure described in this chapter.

Every power-up or reconfiguration event causes the syn1588® VIP Evaluation Board Revision 3 to boot this factory default configuration first. Now it is checked, whether there is a user configuration available as well. If so, the syn1588® VIP Evaluation Board Revision 3 tries to boot this user configuration. Upon success, it remains in this state running the user configuration. The following table shows the basic memory map of the configuration device.

| Range | Description |
|------------------------|-------------------------------|
| 0x0000000 – 0x0c7FFFF | Factory default configuration |
| 0x0c80000 – 0x18FFFFFF | User configuration |
| 0x1900000 – 0x193FFFF | User parameters |

Table 8 Memory map of configuration device

Note, that the factory default configuration uses default parameters while the user configuration loads the previously stored parameters from the non-volatile configuration memory during start-up.

Caution!

If the remote update of a syn1588® VIP Evaluation Board fails e.g. due to high network load immediately re-try the remote update procedure until it successfully completes. Never power down or reboot the unit in this state! This may invalidate the non-volatile!

3.12.1 Pre-Requisites

The following items are required for a successful remote firmware update of a syn1588[®] VIP Evaluation Board Revision 3.

- Oregano Systems' ptpmmm software version 1.4-167 Rev g2975a1f or later
- Optional Oregano Systems' ptpmmm GUI software version 1.3.5 Build 927 or later
- New bitstream (the RPD file) for syn1588[®] VIP Evaluation Board Revision 3 supplied by Oregano Systems' support
- The syn1588[®] VIP Evaluation Board Revision 3 to be updated of course.
- A computer running the ptpmmm software (Windows or Linux)

The syn1588[®] VIP Evaluation Board Revision 3 may be connected point-to-point to the remote update computer or via a switched network.

3.12.2 Remote Firmware Update Procedure – Command Line

The remote update is performed using the ptpmmm management software either by running the ptpmmm on the command line or via the ptpmmm GUI. In the following we will describe in detail the command line flow.

Start the ptpmmm software from the command line as shown in the following example.

```
./ptpmmm
```

First identify the syn1588[®] VIP Evaluation Board Revision 3, which should be updated (e.g using the "clock" command). Determine the clock identifier, the port number and domain of the unit to be updated. See the following example for more details.

```

syn1588(R) PTP Management Tool - IEEE1588-2008
Build date: Jul 25 2017 - V 1.4-167 Rev g2975alf
Copyright (c) Oregano Systems - Design & Consulting GesmbH 2005-2017
Confidential unpublished data - All rights reserved

Command line: ClockID port number
>clock
8CA5A1FFFE00054E 1 OC "IEEE 802.3" 8CA5A100054E IPv4:0A00028B FFFFFFF "Oregano Sy
stems; syn1588(R) VIP; 8C:A5:A1:00:05:4E" "HW build 686; syn1588(R) Clock M 2.3.
2; SW 1.4-42 Rev g71fcd42-dirty" "syn1588_VIP_Rev3.0" 001B19000100
0004A3FFFF327E43 1 OC "IEEE 802.3" 0004A3327E43 IPv4:C0A867EB FFFFFFF "Oregano
Systems; syn1588(R) VIP; 00:04:A3:32:7E:43" "HW build 527; syn1588(R) Clock M
2.1.2; SW 1.2.86" "Oregano test lab" 001B19000100
0004A3FFFF324FF1 1 OC "IEEE 802.3" 0004A3324FF1 IPv4:C0A86775 FFFFFFF "Oregano
Systems; syn1588(R) VIP; 00:04:A3:32:4F:F1" "HW build 527; syn1588(R) Clock M
2.1.2; SW 1.2.86" "Oregano test lab" 001B19000100
0050C2FFFE2DFAE 1 OC "IEEE 802.3" 0050C2C2DFAE IPv4:C0A86702 000F0C "MBG;;"
";;" ";" 001B19000100

```

The update process is initiated by the “update” command. This pre-defined command has been extended with additional parameters.

```

update <ClockId> <PortNumber> <Domain> <rpd-filename> <Startaddr(31:0)>

```

The following example shows such a command. The update process is visualized as a two-step process. “E” characters are displayed while erasing the non-volatile memory and “.” characters are displayed while programming the memory.

3.12.3 Remote Firmware Update Procedure – GUI

Updating the syn1588® VIP Evaluation Board Revision 3' firmware using the ptpmmm GUI is a simple task.

- Invoke ptpmmm GUI
- Select the clock to be updated
- Open the syn1588® VIP firmware update dialog (right click on clock)
- One is asked to select the bit file in the file system (file dialog box)
- One is asked for confirmation for start of the remote update
- A result window is displayed

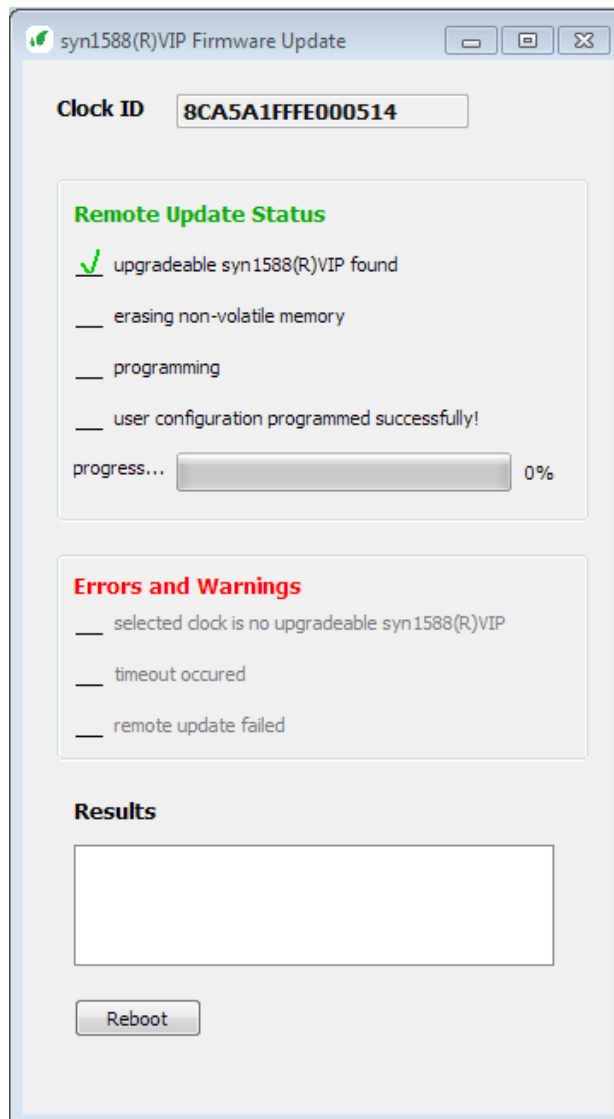


Figure 6 syn1588[®] VIP Evaluation Board – Revision 3: firmware update via syn1588[®] ptpmmm GUI

4 Mechanics

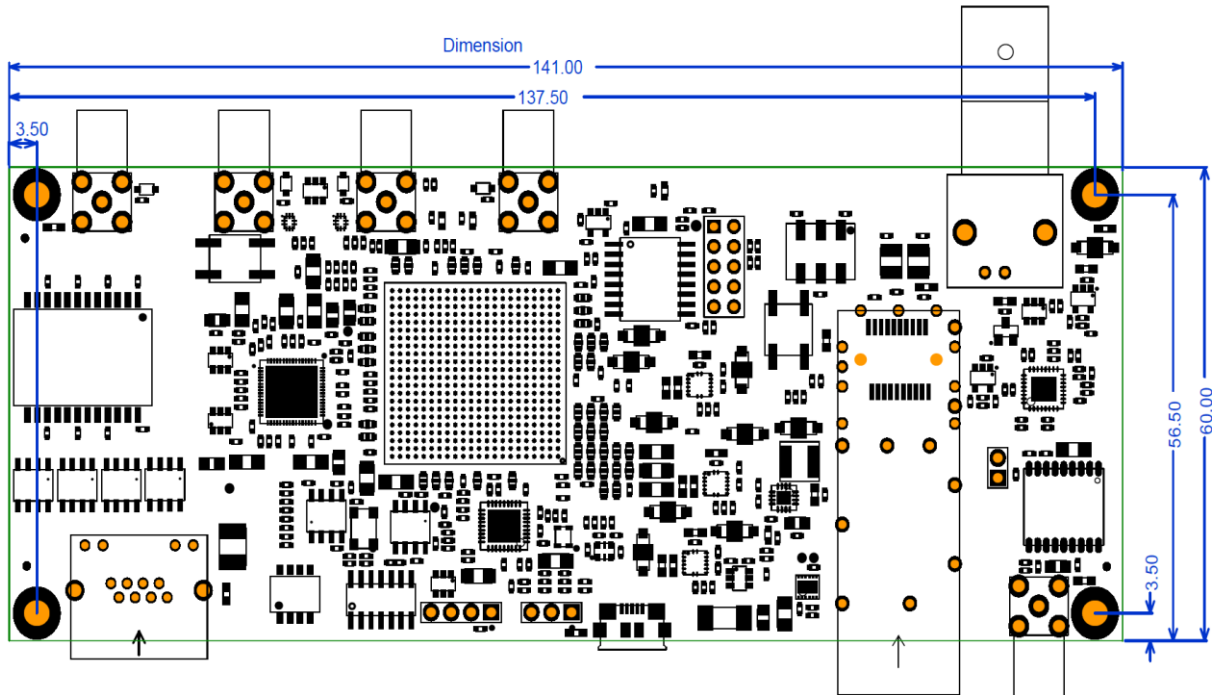


Figure 7 syn1588[®] VIP Evaluation Board – Revision 3: dimensions

5 Electrical Interface Specifications

5.1 ESD

All user accessible connectors of the syn1588[®] VIP Evaluation Board Revision 3 are protected against ESD damage following IEC61000-4-2 15 kV air 8 kV contact. The copper Ethernet interface X1 is additionally protected against lightning following IEC61000-4-4 40 A (5/50 μ s) and IEC61000-4-5 95 A (8/20 μ s) as well as Bellcore 1089 (intra-building) 100 A (2/20 μ s).

5.1.1 Handling Instructions

Caution



The syn1588[®] VIP Evaluation Board is sensitive to electrostatic discharge that may damage the unit. Please observe the proper ESD protection rules. Do not directly touch the syn1588[®] VIP Evaluation Board while not being properly grounded. Use the ESD bags provided by Oregon Systems for shipping and storage.

5.2 Power Supply

The syn1588[®] VIP Evaluation Board Revision 3 can be powered by an USB host device or an USB wall-mount power supply unit. The USB power supply must guarantee a minimum current of 800 mA. A standard-USB 3.x host will be sufficient. The USB-PD (power delivery) standard with voltages other than 5 V and higher currents than 900 mA cannot be used.

If a USB 2.0 host can deliver more than 800 mA, it is also possible to power the syn1588[®] VIP Evaluation Board Revision 3 with it. In this case, the USB power-manager chip on syn1588[®] VIP Evaluation Board Revision 3 will request the maximum current which is possible in the USB 2.0 standard (500 mA). The syn1588[®] VIP Revision 3 board will not limit the supply current to 500 mA. Please notice, that this operation is out of USB 2.0 specification!

For connecting the USB power supply to the syn1588[®] VIP Evaluation Board Revision 3 a standard USB 2.0 cable (type-A / Micro-B connector) must be used. If connecting to an USB 3.1 host with a USB-type C socket, an additional adapter (USB 3.1 type-C / type-A connector) must be used.

5.3 Ethernet: Copper (J5)

The Ethernet interface follows IEEE standard 802.3-2005. The syn1588[®] VIP Evaluation Board Revision 3 supports EEE (Energy Efficient Ethernet aka Green Ethernet) following IEEE 802.3az. This function is deactivated by default and can be activated via the software driver.

5.4 SFP Ethernet Interface (J4)

The SFP interface supports just 1000BASE-X mode using the following SFP transceiver modules.

| Vendor | Type | Mode | Range | Connector | Order Number |
|------------|-------|------------|---------------|-----------|-----------------|
| Fiberstore | fibre | 1000BASE-X | short (550 m) | LC | SFP1G-SX-85 |
| Fiberstore | fibre | 1000BASE-X | long (10 km) | LC | SFP1G-LX-31 |
| Teosco | fibre | 1000BASE-X | short (550 m) | LC | TEO-1.25GSFP-02 |
| Teosco | fibre | 1000BASE-X | long (10 km) | LC | TEO-1.25GSFP-10 |
| Finisar | fibre | 1000BASE-X | short (550 m) | LC | FTRJ-8519 |
| Finisar | fibre | 1000BASE-X | long (10 km) | LC | FTLF1318 |

Table 9 Supported SFP transceiver modules

5.5 SMA User I/Os

There are four user programmable I/Os of SMA type. Every connector may be used for input or output.

The output signals deliver a standard 3V3 level 50 Ω output signal driving a maximum of 20 mA. The input signals expect a standard 3V3 level signal. The output signals may drive two or three standard loads when using correct 50 Ω cabling.

5.5.1 SMA Output Characteristics

| | |
|------------------------------------|-----------------|
| Output coupling | DC |
| Output threshold high | 2.8 V min |
| Output threshold low | 0.4 V max |
| Absolute maximum applied voltage | -0 V to 3.465 V |
| Output to output skew, synchronous | < 1 ns typical |
| Output current | \pm 20 mA max |

Table 10 SMA Output Characteristics

5.5.2 SMA Input Characteristics

| | |
|--------------------------------|---------------------|
| Input impedance | 50 Ω nominal |
| Input coupling | DC |
| Voltage level | 0 to 3.3 V |
| Absolute maximum input voltage | -0.5 V to 4.25 V |
| Minimum pulse width | 500 ns |
| Input threshold high | 2.0 V |
| Input threshold low | 0.8 V |

Table 11 SMA Input Characteristics

5.6 GPS Antenna X1

The syn1588[®] VIP Evaluation Board holds an on-board GPS receiver. This GPS receiver can be connected to a dedicated GPS/GLONASS/BeiDou active antenna to receive GPS/GLONASS/BeiDou satellite signals. The recommended antenna specifications are given in the following table.

| | |
|--------------------|----------------------|
| Antenna Type | active |
| Feeding voltage | 3V3 |
| GPS frequency | 1575.42 \pm 2 MHz |
| GLONASS frequency: | 1602 \pm 4 MHz |
| BeiDou frequency | 1561.098 \pm 2 MHz |
| VSWR | <2 (Typ.) |
| Polarization | RHCP or Linear |
| Gain | > 0dBi |

Table 12 GPS antenna specification

5.7 Production Test

The production test connector must be left unconnected while the syn1588[®] VIP Evaluation Board Revision 3 is operated. Note that there is no special ESD protection for this interface.

6 Environmental

6.1 Temperature

Operating temperature range 0° C ... +50° C

Storage temperature range -40° C ... +85° C

6.2 Humidity

Operating humidity 5% to 80% RH, non-condensing

6.3 Weight

Total weight approx. 90 g (without SFP transceiver)

7 Further Information

You are looking for further information not included in this datasheet? Please contact Oregano Systems support! We will be pleased to provide you all the required information.



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