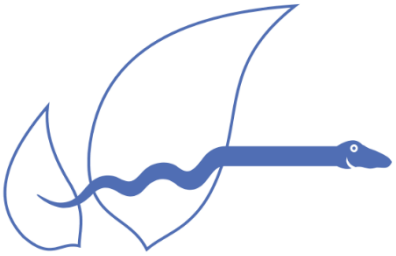

PCI Express Ethernet Network Interface Card

syn1588® Dual NIC

Data Sheet

Version 1.7 – April 20th 2021

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0.1 Contents

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1 Overview

1.1 Functional description

The syn1588® Dual NIC is a standard 100/1000 Mbit PCI Express Ethernet network interface card (1-lane PCI Express low-profile card) offering two SFP type network interfaces with enhancements to provide the network node with accurate clock synchronization via Ethernet following the IEEE1588 standard.

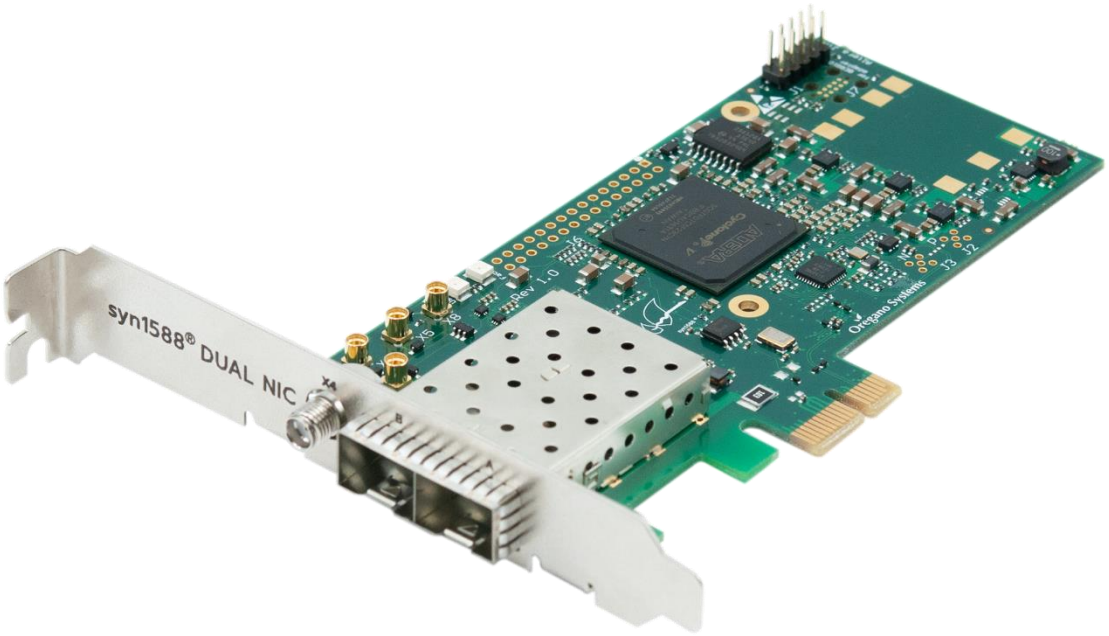

Figure 1: syn1588® Dual NIC

The syn1588® Dual NIC is using the Oregano Systems syn1588® technology for time stamping of arbitrary network packets. The timestamping unit is fully user configurable enabling any type of packet timing application. The syn1588® Dual NIC provides full support for IEEE1588-2008 specific features like the patented on-the-fly timestamping mechanism (one-step mode).

The syn1588® Dual NIC is designed to achieve maximum PTP clock synchronisation accuracy on two network interfaces. Achieving a specific network throughput on these two network interfaces had been no design criteria at all.

Please note, that both hardware clock can be independently operated but they share the common local oscillator clock.

2 Features

2.1 NIC Features

- Standard 100/1000 Mbps Ethernet network card following IEEE802.3-2005
- Two SFP type network interfaces
- SFP transceiver modules 100BASE-TX ,1000BASE-X and 1000BASE-T supported
- 1-lane PCI Express (PCIe) low-profile card
- Compliant to PCI Express version 2.0 (5 Gbit/s)
- Compatible with PCI Express version 1.1 (2.5 Gbit/s)
- 4 kByte Ethernet transmit FIFO, 16 kByte Ethernet receive FIFO
- VLAN and IPv6 support
- Promiscuous mode supported
- one user programmable SMA connectors
- Driver software currently available for Linux only. Both 32 bit and 64 bit systems are supported.

2.2 IEEE1588 Features[1]

- Fully IEEE1588-2008 & IEEE1588-2019 compliant
- Support for Oregano Systems' patented syn1588® technology:
- On-the-fly timestamping while sending or receiving time sync packets (1-step mode)
- IEEE1588 hardware clock - the IEEE1588 clock is fully maintained in hardware
- Clock servo operation is controlled by the software without real-time requirements
- IEEE1588 hardware clock utilizes IEEE1588 time format
- Software does not need to run time format conversions
- syn1588® clock frequency is 125 MHz
- All real-time functions for IEEE1588 are implemented in hardware eliminating real-time constraints for the syn1588® PTP Stack
- IEEE1588 master and slave operation supported[2]

[1] Requires the Oregano Systems syn1588® PTP Stack to run the protocol engine.

[2] Oregano Systems generally recommends using the OCXO option for all master applications.

- High quality TCXO oscillator (better than 1.5 ppm)
- Optional high-stability OCXO oscillator (better than 0.5ppm)
- 1 PPS output signal[3]
- One pulse per second, rising edge, if seconds wrap in the IEEE1588 hardware clock
- Programmable interrupt conditions
- one programmable input/output signal available on SMA connectors (50 Ω, 3V3 LVCMOS signal level):
- EVENT input
- TRIGGER output
- PERIOD output
- IRIG-B007 output data stream generation
  (DCLS signal, no carrier, BCD + BCD_Year + SBS)
- Optional IRIG-B007 input decoding
  (DCLS signal, no carrier, BCD + BCD_Year)
- On-board jitter cleaner PLL for generating accurate, synchronized single-ended frequencies up to 156.25 MHz
- Connectivity to an external GPS receiver via the 1 PPS input as well as a serial port of the host PC for external synchronization
- Serial port not included in the syn1588® Dual NIC, NMEA-0183 RMC messages required
- Binary run-time license for syn1588® PTP Stack included
- Several utilities are available for accessing registers, synchronizing the node's system clock, or synchronizing to an external GPS receiver.
- Software APIs are available allowing the user to write custom software including interrupt service routines accessing the syn1588® functions, accessing all hardware clock related functions and controlling/observing the syn1588® PTP Stack
- syn1588® Linux Live System for fast testing of the syn1588® Dual NIC without the need of software installation. Just install the syn1588® Dual NIC in your node and boot the PC using the syn1588® Linux Live System

[3] Constant delay of three clock periods to the external output signal. Minimum pulse width is 100 µs.

2.2.1 Timestamping

- Programmable timestamping unit on Ethernet receive and transmit path for time stamping IEEE1588 packets
- Independent timestamp FIFOs for Ethernet receive path (256 words) and Ethernet transmit path (16 words) allows timestamping of multiple dense packets without losing data thus removing the software real-time requirements
- Patented on-the-fly timestamping for 1-step operation on Ethernet transmit path
- 1-step timestamping just supported for 100 Mbit and 1000 Mbit full duplex operation
- Timestamping supported for VLAN as well as IPv6 operation
- Timestamping of external input signal – EVENT: On the rising edge of these external signals a timestamp will be drawn
- For EVENT0 input a 16 entry timestamp FIFO is implemented allowing timestamping of dense events with a distance of just 100 ns
- Extremely high timestamp resolution of 5 ns

2.2.2 User Programmable Events

- TRIGGER: one user programmable single event output signal may be generated
- This TRIGGER changes the respective state of the output signal at a programmable time that is derived from the high-accuracy IEEE1588 hardware clock
- TRIGGER0 output is controlled by a 16 entry FIFO providing support for dense event sequences without imposing real-time requirements on the software
- Resolution of TRIGGER events is +/-5 ns
- Maximum TRIGGER event duration is 32 bit seconds
- PERIOD: one user programmable periodical output signals may be generated that are derived from the highly accuracy IEEE1588 hardware clock
- The frequency may be selected in the range of mHz to 156.25 MHz
- The resolution of the PERIOD event is 2^{-16} ns, i.e. 0,0153 ps
- The maximum PERIOD duration is 65535 seconds (16 bit)

Both syn1588®Clock_M IP cores (one assigned for each network interface) have to share a common set of one external SMA IO and three internal SMA IOs (available with the PLUG option). The user is responsible for selecting just one function of either of the two syn1588®Clock_M IP cores to the SMA IOs. In case of collisions the assignment for the second interface will supersede.

2.3 Hardware Options

- High precision OCXO (0.05 ppm) for master operations or high accuracy applications.
- 3 additional internal SMA connectors (Plug option)

3 Block Diagram

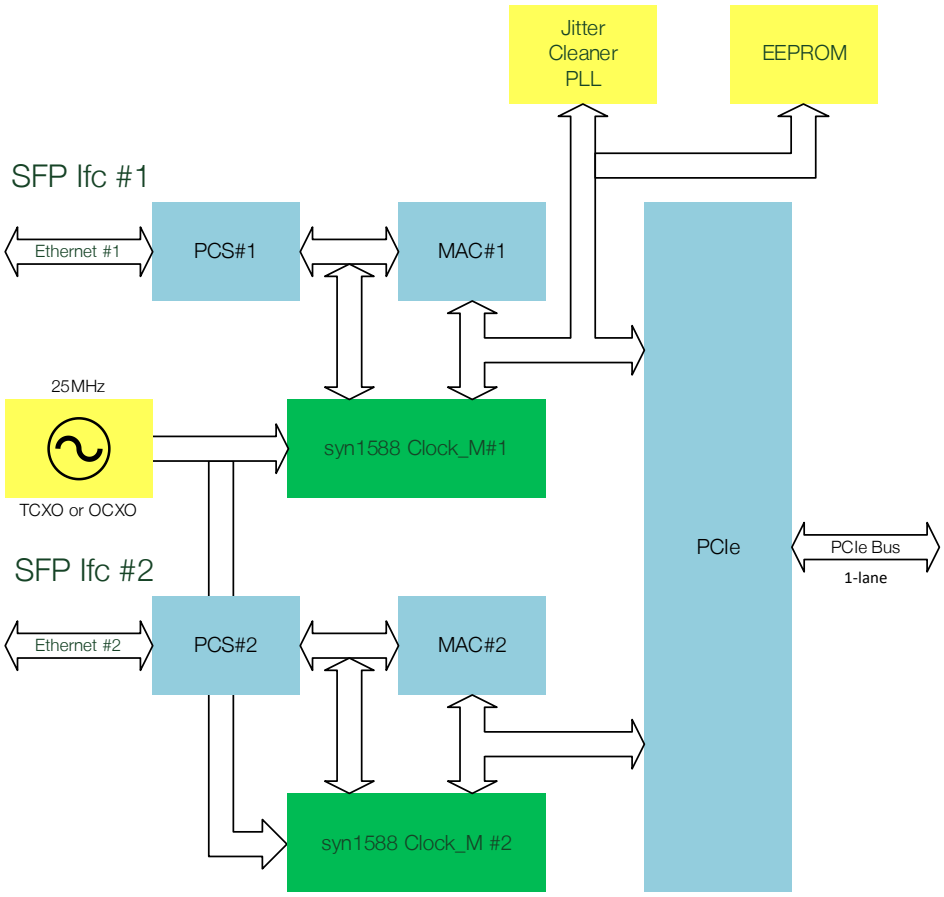

Figure 2: syn1588® Dual NIC: block diagram

The syn1588® Dual NIC basically consists of a single FPGA containing the following IP cores:

- 100/1000 Mbps Ethernet Media Access Controller (MAC)
- syn1588® Clock_M IP Core
- PCS/PMA function for SFP type network interface
- PCIe interface

The following figure shows the two network interfaces. Each network interface is assigned an independent syn1588® PTP hardware clock function (syn1588Clock_M IP core).

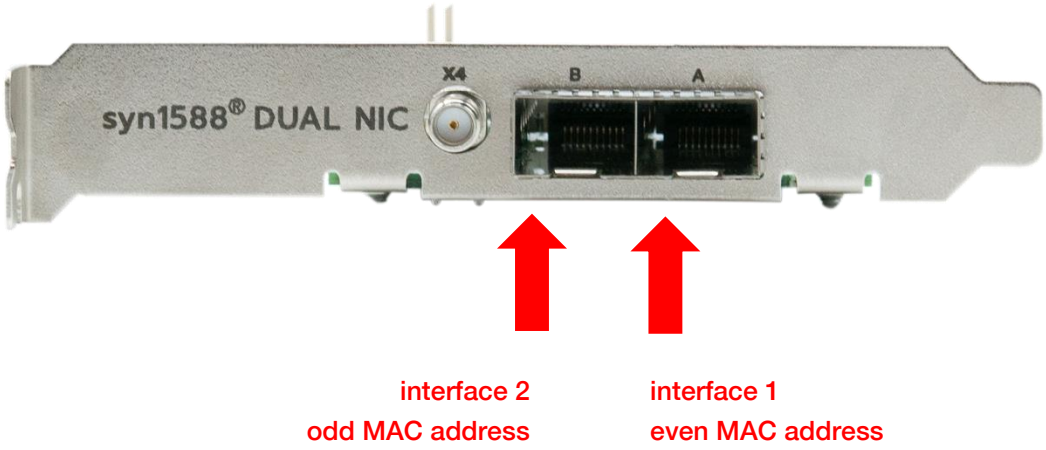

Figure 3: syn1588® Dual NIC: network interfaces

The first network interface is assigned an even MAC address while the second network interface is assigned an odd MAC address. All board related functions like jitter cleaner PLL, MAC address and serial number EEPROM etc. can just be addressed via the first network interface.

4 Function

The syn1588® Dual NIC comes as default with the function of two independent network interfaces each enhanced with high-accuracy PTP functions. The syn1588® Dual NIC hardware may also act as a hardware platform for other functions like HSR and PRP (IEC 62439 3 standard) as well. These functions are currently just available for selected customers upon request

5 Mechanics

The following figure shows the dimensions of the syn1588® Dual NIC.

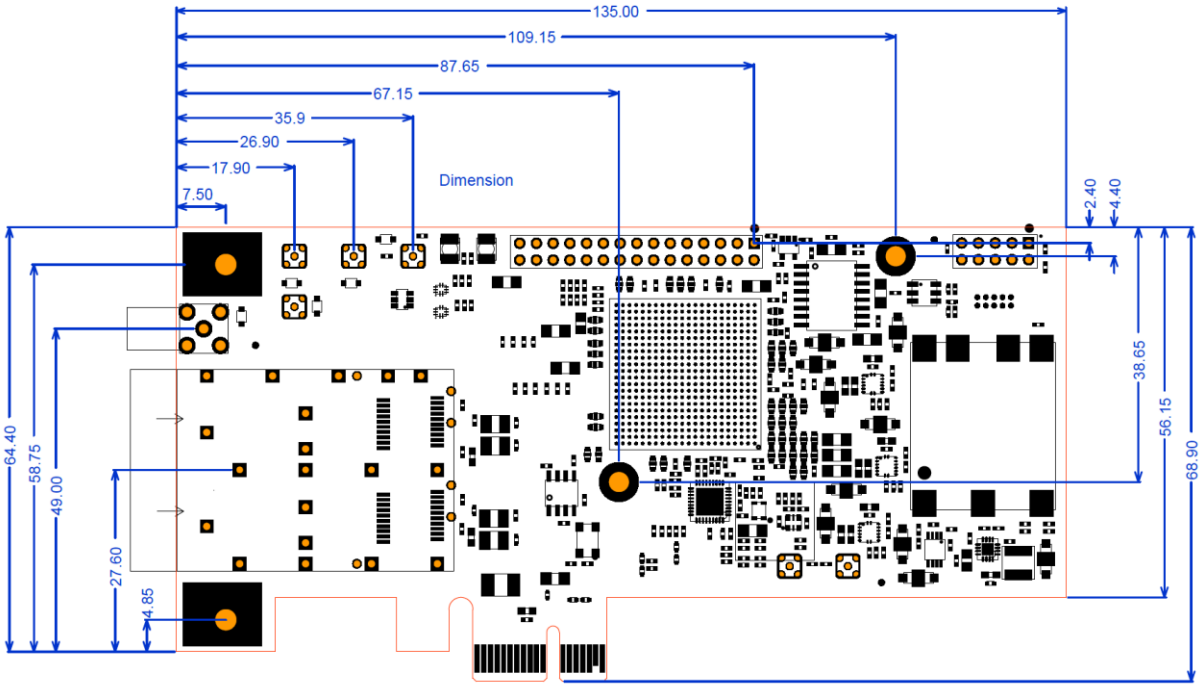

Figure 4: syn1588® Dual NIC: dimensions & placement of connectors (all dimensions are in mm)

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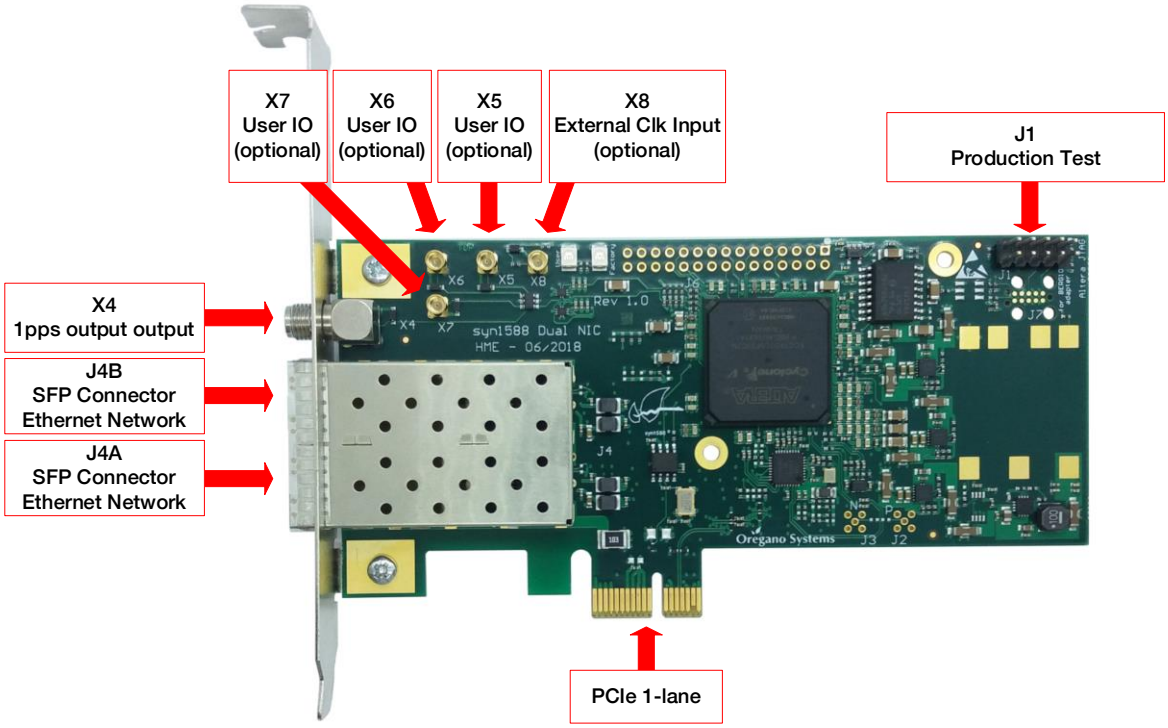

Figure 5: syn1588® Dual NIC: connectors

6 Electrical Interface Specification

6.1 ESD

All user accessible connectors of the syn1588® Dual NIC are protected against ESD damage following IEC61000-4-2 15 kV air 8 kV contact.

6.2 Power Supply

The syn1588® Dual NIC board is operated using the 3V3 power supplied by the PCI Express edge connector. The oscillators – the TCXO as well as the optional OCXO - are powered by highly stable on-board supply which uses the 12V supplied by the PCI Express edge connector.

DC Characteristics	
Minimum DC 3V3 input voltage	3.0 V
Maximum DC 3V3 input voltage	3.6 V
Maximum DC supply current @ 3,3 V	1.0 A
Minimum DC 12V input voltage	11.5 V
Maximum DC 12V input voltage	12.5 V
Maximum DC supply current @ 12V	0.2 A

Table 1 Power supply DC characteristics

6.3 SFP Ethernet Interfaces (J4A & J4B)

The SFP interface supports 100BASE-X, 1000BASE-X and 1000BASE-T mode using the SFP transceiver modules listed in Table 2. While other SFP transceiver modules might work as well, we cannot guarantee their function.

Vendor	Type	Mode	Range	Connector	Order Number
Avago	fiber	1000BASE-X	short (550 m)	LC	AFBR-5710PZ
Avago	fiber	1000BASE-X	long (10 km)	LC	AFCT-5710PZ
Fiberstore	fiber	1000BASE-X	short (550 m)	LC	SFP1G-SX-85
Fiberstore	fiber	1000BASE-X	long (10 km)	LC	SFP1G-LX-31
Finisar	fiber	1000BASE-X	long (10 km)	LC	FTLF1318
Fiberland	fiber	1000BASE-X	short (550 m)	LC	FLD-SG-MMD-1
Fiberland	fiber	1000BASE-X	long (10 km)	LC	FLD-SG-SMD-10
Fiberland	copper	100BASE-TX 1000BASE-T	100 m	RJ45	FLD-SASG-T

Table 2 Supported SFP transceiver modules

All fiber SFP transceiver modules use the LC connector. Using the SR module (850nm) one achieves at least 300 m connection distance using a 62.5/125m MMF. Using the LR module (1310nm) one achieves 10 km connection distance using a 9/125m SMF.

By default, the card comes with two short range 1000BASE-X SFP transceiver modules.

6.4 User Interface (X4 – X7)

There are four connectors available for the user; one SMA connector at, the PCI bracket and three MMCX connectors internally. Each connector is configurable as input or output for every implemented signal.

Input signals:

- event_0
- event_1
- irigb_input

Output signals:

- 1PPS
- period_0
- period_1

- period_2 (light)
- period_3 (light)
- trigger_0
- trigger_1
- irigb_output
- framesync
- Jitter-Cleaner-PLL

The default configuration is: two input and two output signals.

- X4: 1 PPS
- X7: period_0 output signal
- X6: event_0 input signal
- X5: disabled

Note, both syn1588®Clock_M IP cores (one assigned for each network interface) have to share this common set of IOs. The user is responsible for selecting just one function of either of the two syn1588®Clock_M IP cores/network interfaces to the SMA IOs. E.g. just any of the two 1PPS signals can be routed out at the same time on the same IO connector.

In case of collisions the assignment for the second interface will supersede. All board related functions (like jitter-cleaner PLL) is just available for the first network interface/ syn1588®Clock_M IP core.

The output signals deliver a standard 3V3 level 50 Ω output signal driving a maximum of 20 mA. The input signals expect a standard 3V3 level signal. The output signals may drive two or three standard loads when using correct 50 Ω cabling.

One SMA connectors (X4) is directly available at the PCI bracket while three more connectors (X5, X6 and X7) are available internally. Upon request (via the appropriate ordering code) Oregano Systems supplies the cable to directly connect to a SMA port.

6.4.1 SMA Output Characteristics

Output coupling	DC
Output threshold high	2.8 V min
Output threshold low	0.4 V max
Absolute maximum applied voltage	-0 V to 3.465 V
Output to output skew, synchronous	< 1 ns typical
Output current	±20 mA max

Table 3 SMA Output Characteristics

6.4.2 SMA Input Characteristics

Input impedance	50 Ω nominal
Input coupling	DC
Voltage level	0 to 3.3 V
Absolute maximum input voltage	-0.5 V to 4.25 V
Minimum pulse width	500 ns
Input threshold high	2.0 V
Input threshold low	0.8 V

Table 4 SMA Input Characteristics

6.5 External clock Input Interface (X8)

Optionally there is an external clock input available to allow direct driving the syn1588® hardware clock from this external signal.

Input impedance	50 Ω nominal
Input coupling	DC
Voltage level	0 to 3.3 V
Absolute maximum input voltage	-0.5 V to 4.25 V
Input threshold high	2.0 V
Input threshold low	0.8 V

Table 5 External Clock Input Characteristics

6.6 Production Test (J1)

The production test connector must be left unconnected while the syn1588® Dual NIC is operated. Note that there is no special ESD protection for this interface.

7 Environmental

7.1 Temperature

Operating temperature range	0° C ... +50° C
Storage temperature range	-40° C ... +85° C

7.2 Humidity

Operating humidity 5% to 80% RH, non-condensing

7.3 Weight

Total weight approx. 70 g (without OCXO)

Total weight approx. 75 g (with OCXO)

8 Installing the syn1588® Dual NIC Hardware

The following instructions are general installation guide lines. Consult your computer's user manual for specific instructions and warnings for installing new PCI/PCIe components.

Caution

The syn1588® Dual NIC is sensitive to electrostatic discharge that may damage the unit. Please observe ESD protection rules. Do not directly touch the unmounted syn1588® Dual NIC while not being properly grounded. Use the ESD bags provided by Oregano Systems for shipping and storage.

8.1 Installation

- Be sure to have powered–off your PC prior to installing the syn1588® Dual NIC. Failure to do so could endanger you and may damage the syn1588® Dual NIC or computer

- Please be sure to thoroughly ground yourself by means of a grounding strap or by touching a grounded object prior to unpacking the syn1588® Dual NIC card

- Insert the syn1588® Dual NIC into the empty PCIe slot and verify that the card is properly inserted and fastened by means of levels or screw of the case

- Plug in the power cord of the computer and power the computer on

The syn1588® Dual NIC card is now installed.

Caution

Please note that some BIOS implementations do not allow plugging a 1-lane PCIe card into an 8-lane or 16-lane slot. Please consult your BIOS manual in case of troubles.

9 Software

9.1 Driver

The syn1588® Dual NIC requires a driver software for its operation on your host PC. There are drivers available for Linux for both 32 bit and 64 bit systems. Currently, the following operating systems are officially supported.

OS
Linux kernel version 2.6.32 – 5.0.*

Table 6 Driver software: supported OS

Please consult the syn1588® User Guide or the Quick Start Guide Application Note for further installation instructions.

Please be aware that the current driver versions do not support any power-saving mode like stand-by or hibernation. The syn1588® Dual NIC needs to be restarted by reloading the driver.

9.2 syn1588® PTP Stack

Every syn1588® Dual NIC comes with a binary run-time license of the syn1588® PTP Stack. The syn1588® PTP Stack is available for both Windows and Linux. The syn1588® PTP Stack supports all operating system versions listed in Table 6 Driver software: supported OS

Please refer to the syn1588® User Guide for more information on using syn1588® software.

10 Further Information

You are looking for further information not included in this datasheet? Please contact Oregano Systems support! We will be pleased to provide you all the required information.

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Vienna, January 20th 2021

RoHS Certificate of Conformance

The Oregano Systems' syn1588® products listed below is (are) in compliance with Directive 2011/65/EC and 2015/863/EC on the restriction of the use of certain hazardous substances in electrical and electronic equipment (RoHS and RoHS 3 directives).

- syn1588® Gbit Switch (board revision 1.7)
- syn1588® PCIe NIC Revision 2.1
- syn1588® VIP Evaluation Board Revision 3
- syn1588® Dual NIC Revision 1.0

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Vienna, April 19th 2021

WEEE status of the product

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RL 94/62/EG status of the packaging material

This packaging material is handled as a B2B category packaging material. In order to secure a RL 94/62/EG compliant waste disposal it has to be returned to the manufacturer. Any transportation expenses for returning this product have to be incurred by the end user, whereas Oregano Systems will bear the costs for the waste disposal itself.

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Vienna, January 20th 2021

Letter of Volatility

The following table shows the non-volatile memories of the syn1588® Dual NIC – Revision 1.0. Please note that no customer data is stored in these non-volatile memories.

memory	function	size	writeable	user R/W	access restriction
SPI Flash U17 Micron N25Q2128A13ESF40G	FPGA configuration storage	128Mbit	yes	no	dedicated firmware update software required, only user configuration may be written, factory default configuration is write protected in hardware
I2C EEPROM U1 ON Semiconductor CAT24AA01TD	MAC address	1kbit	no	no	no write access implemented in hardware

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