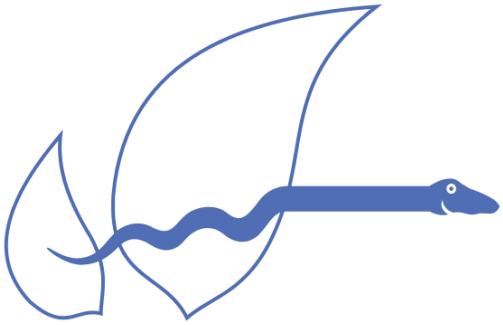

syn1588 ®

Single Chip IEEE1588 Clock Synchronization Solution

syn1588® VIP IP Core

Data Sheet

Version 1.10 – March 21st 2019

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0.1 Contents

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1 Overview

The syn1588® VIP IP Core provides a cost effective highly integrated single chip IEEE1588 solution. Only an external Ethernet physical layer IC (PHY) is required to create a fully functional layer2 or layer3 IEEE1588node.

The syn1588® VIP is equipped with a standard 10/100/1000 Mbit/s MII/GMII Ethernet network interface with enhancements for highly accurate clock synchronization via Ethernet following the IEEE1588-2008 standard. The entire clock synchronization operation is implemented on an on-chip microcontroller executing the complete PTP Stack. No external memory components are needed resulting in a fully self-contained implementation of the IEEE 1588-2008 standard.

Furthermore, the UART outputs a GPS compatible NMEA data stream. Thus the syn1588® VIP can be easily used as GPS replacement to distribute GPS time in a LAN.

1.1 Block Diagram

Figure 1 shows the block diagram of the syn1588® VIP IP core. The syn1588® VIP IP core requires merely an external Ethernet Physical Layer IC. The IP core is connected to a clock source, typically a 25 MHz low cost 50 ppm crystal oscillator. One may use the same XO for this purpose that is required for the Ethernet PHY.

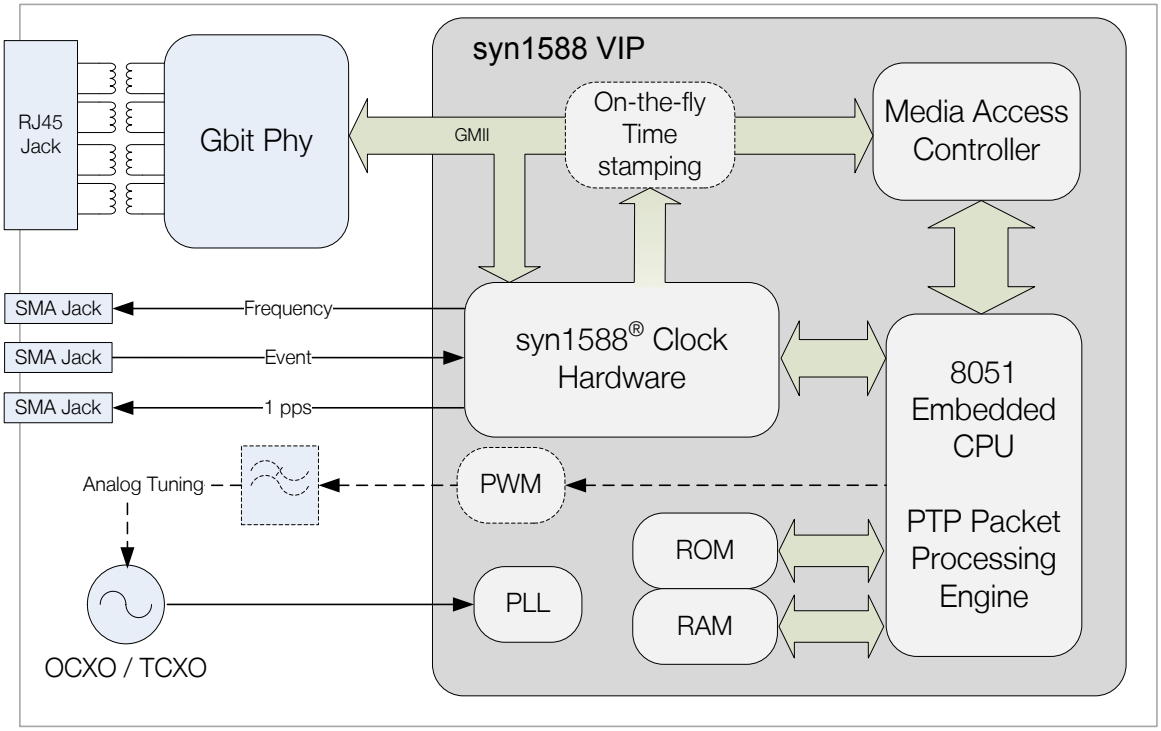

Figure 1 Block diagram: syn1588® VIP

1.2 Ordering Information

The syn1588® VIP IP Core can be ordered directly from Oregano Systems or via our distributors (see http://oregano.at for details). There are several options of the syn1588® VIP IP Cores available.

syn1588 VIP-ipcore-<type>

- Source code license
  order code <type> equal to “src”
- FPGA technology netlist license
  order code <type> equal to “fpga”
  This option additionally requires the specification of the target FPGA technology.

2 Features

The syn1588® VIP offers the following features

2.1 General

- Fully IEEE1588-2008 standard compliant network node in a single chip
- Single chip solution (except the external Ethernet PHY and one oscillator)
- Support for 10/100/1000 Mbit/s operation (GMII mode) following the IEEE802.3-2005 standard
- Typical clock accuracy better than 50 ns

2.2 IEEE1588

- syn1588®PTP stack binary included (running on integrated 8-bit CPU core)
- syn1588® VIP acts as master or slave following IEEE1588-2008
  - user may select either BMC mode or dedicated mode
- supported sync rates: -6 to 6
- supported delay request rates: -2 to 8 (relative to sync rate)
- IEEE1588-2008 two-step clock mode supported
- IEEE1588-2008 one-step clock mode supported
- IEEE1588-2008 multicast mode supported in default firmware version
- IEEE1588-2008 unicast mode optionally supported using a custom firmware option
- IEEE1588-2008 network layer 3 (Internet Protocol) supported in standard configuration
- IEEE1588-2008 network layer 2 optionally supported using different firmware version

2.3 Interface & IO

- The syn1588® VIP device delivers a 1PPS signal
- The syn1588® VIP delivers a frequency output signal with a user selectable frequency in the range from 1 mHz to 5 MHz
- The syn1588® VIP offers an event input
  - May be used for 1PPS input received from a GPS
- The syn1588® VIP offers a UART output
  - Output of time information in GPS compatible NMEA format suited for GPS replacement via LAN
  - Output of status information of syn1588®PTP stack
- Supported Ethernet PHYs
  - Marvell 88E1111
  - Micrel KSZ9021/KSZ9031
- There are four mode select input signals
  - May be used for custom firmware versions
- There is a “In-Sync” output signal (high active)

2.4 Remote Management

- PTP management interface is supported ([IEEE 1588-2008] Clause 15) allowing remote management and remote update
- Dual boot capability: factory default firmware and user firmware
- Remote update of user firmware
- Remote management of syn1588® VIP parameters

3 Functional Description

The syn1588® VIP device is entirely self-contained and does not need any user interaction to operate. Via the PTP management interface status information can be gathered in layer 3 mode and clock parameters as well as I/O options can be configured.

3.1 Principal Operation

After power up or whenever the device is reset it starts polling the Ethernet PHY's link status to decide between MII or GMII operation. In parallel the syn1588® VIP start reading its parameter set from the non-volatile memory (SPI Flash). If no valid parameter set is found, the factory default parameter settings of the firmware are used.

After fetching a MAC address from the I2C device IEEE1588 PTP operation is started by trying to connect to an IEEE 1588 Master via the network. If no master is found and the syn1588® VIP is not explicitly configured as a slave the device will become master after a certain time as specified in the IEEE1588 standard.

The syn1588® VIP IP core's interface is made up of a two-level hierarchy.

- syn1588 VIP_core
- syn1588 VIP_top

The "syn1588 VIP_top" unit corresponds to the interface of the syn1588® VIP device. It is made up an instance of the "syn1588 VIP_core" unit, the required PLLs as well as the clock detection and clock switching function. The "syn1588 VIP_core" unit offers some additional interface signals that might be useful when embedding the syn1588® VIP in a SoC design. This includes the information, whether an Ethernet network link has been established, the in-sync signal, the access to the syn1588® hardware clock and the microprocessor's port signals. Latter one allows custom specific hardware/software interactions.

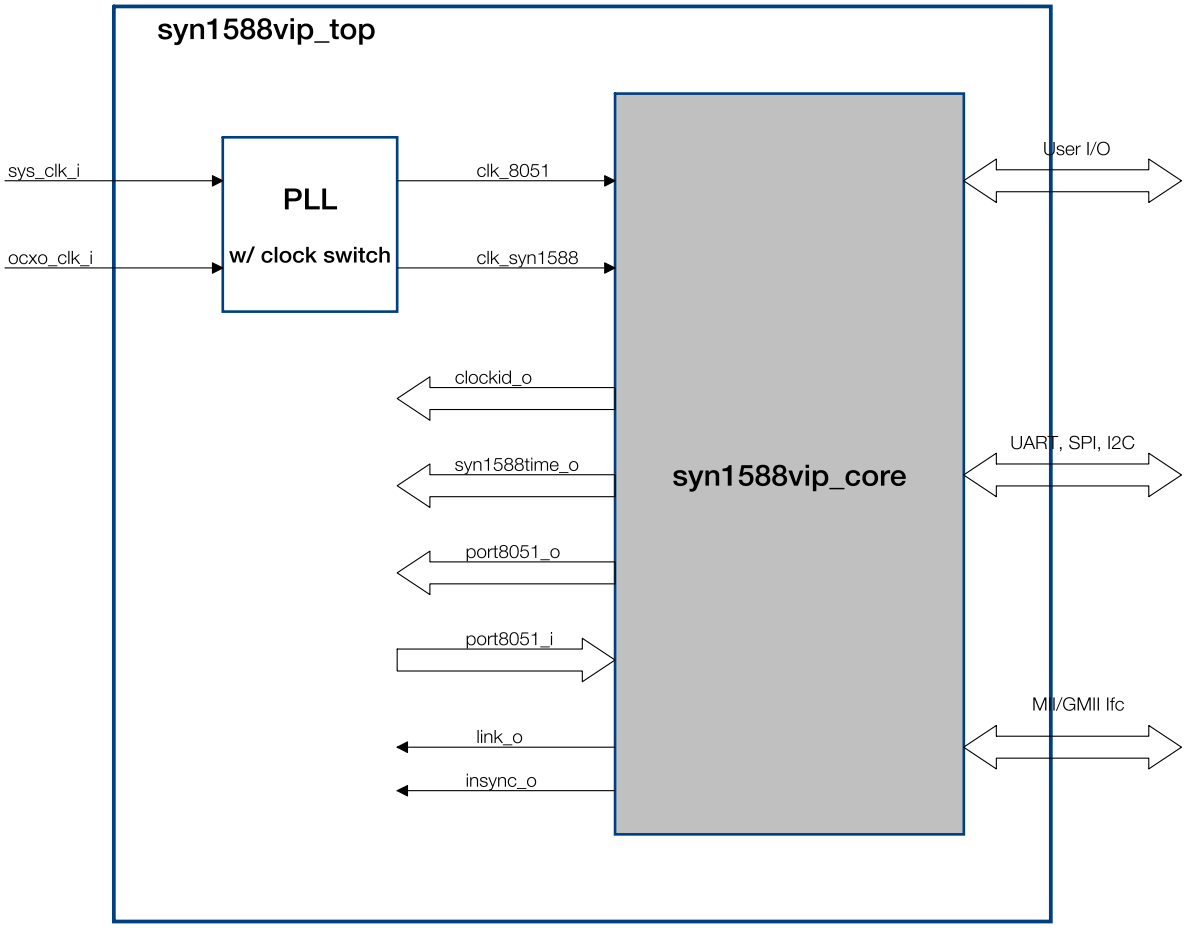

Figure 2 syn1588® VIP design hierarchy

The "syn1588 VIP_top" unit is intended for users that intending to implement the syn1588® VIP's function in a single device (ASIC or FPGA). If one would like to embed the syn1588® VIP in context with other logic one can use the "syn1588 VIP_core" unit.

3.2 User I/Os

There are three I/Os - two outputs and one input - for user application purposes.

- 1PPS output
- event input
- frequency output

3.2.1 1PPS / IRIG-B Output

The 1PPS signal is available on the output signal "onepps_o". A rising edge is output once every second. The pulse width is minimum 1 us. The delay of the rising edge with respect to the wrap of the second is three clock periods of the 100 MHz syn1588® clock frequency, i.e. 30 ns.

Right after initialization the 1PPS output will start to operate if the mode select signal mode_sw_i(2) is active (i.e '1').

If the mode select signal mode_sw_i(2) is inactive (i.e '0') the IRIG-B function is selected to be output on the 1PPS pin.

3.2.2 Event Input

The EVENT input is available at the input signal "event_i". A signal transition from low-to-high (rising edge) of an external signal (e.g. a sensor value reaching a threshold) will be sampled with the 100 MHz syn1588® clock, a time stamp will be drawn and stored in a local buffer memory. For the correct sampling the minimum pulse width of the external signal has to be three clock periods of the 100 MHz syn1588® clock frequency, i.e. 30 ns.

3.2.3 Frequency Output

The frequency output signal is available at the output signal "frequency_o". The user may generate an arbitrary frequency derived from and phase locked to the synchronized, high accuracy clock with a resolution of 1 mHz (0.001 Hz) and below. Please keep in mind that frequencies generated by means of the syn1588® VIP period output will be phased locked on all nodes within a synchronized IEEE1588 network regardless of the value of the frequency.

The frequency output signal will be instantaneously available if the syn1588® VIP operates in master mode. In slave mode the frequency output is available if a master is present in the network and the offset of the node to the master is less than 10 us for the last 16 sync periods.

3.3 Accuracy

The overall accuracy within an IEEE1588 network or in other words the maximum deviation between the 1PPS clock signals of any two given nodes is both dependent on several different configuration parameters and on the hardware of the nodes itself.

The latter has two major aspects to consider: On the one side the resolution of the high accuracy IEEE1588 clock located at the network interface defines the resolution of the time stamps gathered will scanning for IEEE1588 timing related packets. Furthermore the stability of the oscillator driving the high accuracy clock is of equal importance when evaluating accuracy.

With respect to configuration parameters the rate of the sync and, to a certain extent, the rate of the delay request packets have considerable impact on the overall accuracy. For more details please refer to the white paper on highly accurate clock synchronization authored be Oregano Systems.

The local clock of the syn1588® VIP chip offers a resolution of less than 10 ns. If it is equipped with a 50 ppm 25 MHz oscillator accuracy in the range of some ±100 ns can be achieved if the message rate is selected in the range of 1 sec.

4 Interface Description

4.1 MII/GMII Interface

The Ethernet physical layer device is connected to the syn1588® VIP IP core via a standard GMII interface. The interface operates at 2.5 MHz, 25 MHz, or 125 MHz respectively according to the negotiated link speed.

If the GMII interface mode is not used the unused inputs, i.e. gmii_rxd_i<7:4>, should be tied to GND. The unused outputs, i.e. gmii_txd_o<7:4> should be left open.

4.2 Clock Inputs

The syn1588 VIP_top unit requires either the sys_clk_i or the ocxo_clk_i clock as input. Both clocks are expected to be 25 MHz with 50% duty cycle. A PLL generates out of the selected input clock the two clock signals clk_8051_i driving the processor and clk_syn1588_i operating the syn1588® hardware clock. The maximum frequency of these two internal clocks depends on the selected target technology. When using the syn1588 VIP_core unit one may use any input frequency to generate the two internal clock signals.

After power up or after a reset a state-machine implemented in syn1588 VIP_top will search for a valid clock signal in the ocxo_clk_i input pin. If an appropriate clock is found the syn1588® hardware clock is from that point on clocked with the 25 MHz clock signal in the ocxo_clk_i pin, otherwise the 25 MHz sys_clk_i input pin is used. Note that proper clock switch-over and PLL setup is all implemented in the syn1588® VIP chip.

Requirements for the MII/GMII clock inputs can be found in Section 3.3.

4.3 I2C Interface

A standard I2C interface is provided to hook up a ROM containing the MAC address for the device. An example for a compatible device is the Microchip[1] 24AA02E48.

4.4 Reset

The input signal reset_n_i allows to reset all registers of the syn1588® VIP IP core. It does not clear the internal SRAM memory cells, which are only cleared with a power cycle.

There is a reset output signal available reset_n_o that is driven by the internal watchdog unit. This open collector signal may be used as a reconfiguration signal for the FPGA that implements the syn1588® VIP function.

[1] See http://www.microchip.com for further information.

4.5 UART Interface

A serial interface for status information output is available. The interface operates at 115200 baud with no parity, one stop bit, and no handshake.

NMEA 0183 (or NMEA for short) is a combined electrical and data specification for communication between marine electronic devices such as gyrocompass, autopilot, GPS receivers. The GPRMC-Dataset (RMC = recommended minimum sentence C) is recommenced as the minimum support of a GPS receiver.

```
$GPRMC,191410,V,0.0,N,0.0,E,0.0,0.0,100210,0.4,E*19
       ^      ^ ^   ^     ^   ^   ^      ^     ^
       |      | |   |     |   |   |      |     |
       |      | |   |     |   |   |      |     New in NMEA 2.3:
       |      | |   |     |   |   |      |     Mode of operation
       |      | |   |     |   |   |      |     A=autonomous
       |      | |   |     |   |   |      |     D=differential
       |      | |   |     |   |   |      |     E=estimated
       |      | |   |     |   |   |      |     N=not valid
       |      | |   |     |   |   |      |     S=simulator
       |      | |   |     |   |   |      |
       |      | |   |     |   |   |     Variation
       |      | |   |     |   |   |
       |      | |   |     |   |  Date: 10.02.2010
       |      | |   |     |   |
       |      | |   |     |  Direction in degrees
       |      | |   |     |
       |      | |   |    Velocity over ground
       |      | |   |
       |      | |  Longitude with direction (E=East, W=West)
       |      | |
       |      | |
       |      | Latitude with direction (N=North, S=South)
       |      |
       |      |
       |     Status: A=Active; V=void
       |
      Time: 19:14:10 (UTC-Time)
```

This capability allows a set of syn1588® VIP devices to replace GPS receivers by distributing timing information of a single GPS receiver across a LAN.

4.6 SPI Flash Memory Interface

An external SPI flash memory may store firmware versions when implementing the syn1588® VIP IP core into a FPGA. The syn1588® VIP IP core supports two firmware configurations of the syn1588® VIP:

- Factory default configuration
- User configuration

Latter one may be updated during normal operation. Additionally, the SPI flash enables non-volatile storage of the syn1588® VIP's parameters set by the user. The syn1588® VIP supports the following Flash memory device from Microchip (formerly SST):

- SST25VF032B

The datasheet may be found at: http://www.microchip.com . The following figure shows how the SPI Flash memory shall be connected to the syn1588® VIP.

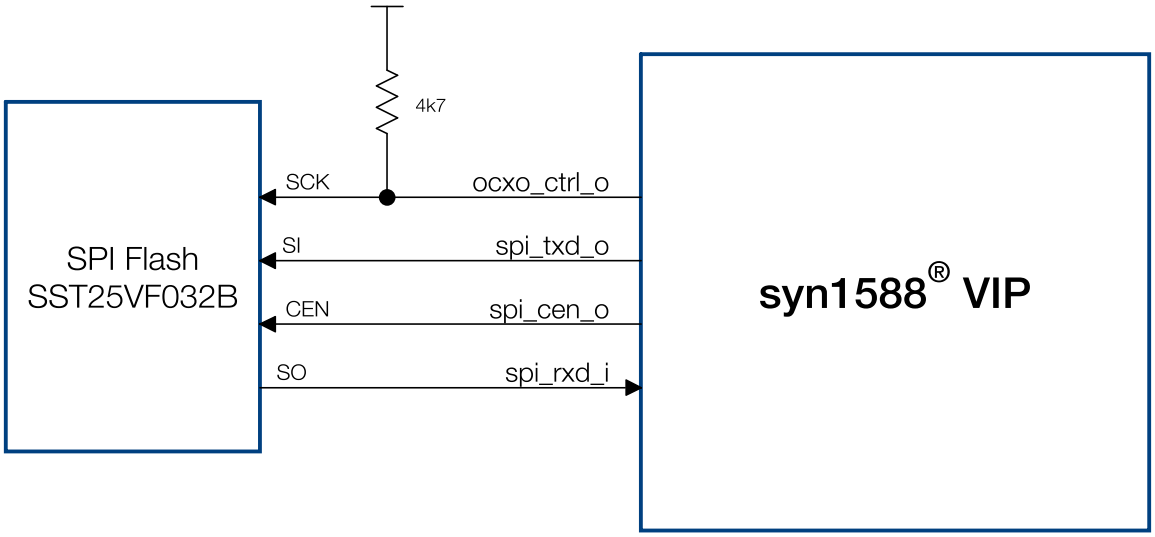

Figure 3 Connecting the SPI flash to the syn1588® VIP

4.7 Mode Select Interface

There are four mode select signals controlling the basic mode of operation of the syn1588® VIP.

- mode_sw_i(2:0)

The mode_sw_i(2) signal selects the 1PPS function (when active or '1') or the IRIG-B function (when inactive or '0') to be output on the 1PPS pin.

The signals mode_sw_i(0) and mode_sw_i(1) are currently unused and reserved for future use.

4.8 Voltage controlled OCXO

The syn1588® VIP supports voltage controlled OCXO to further increase the accuracy. The standard firmware supports static values of the OCXO control voltage. The following diagram shows the recommended connection of such a voltage controlled OCXO.

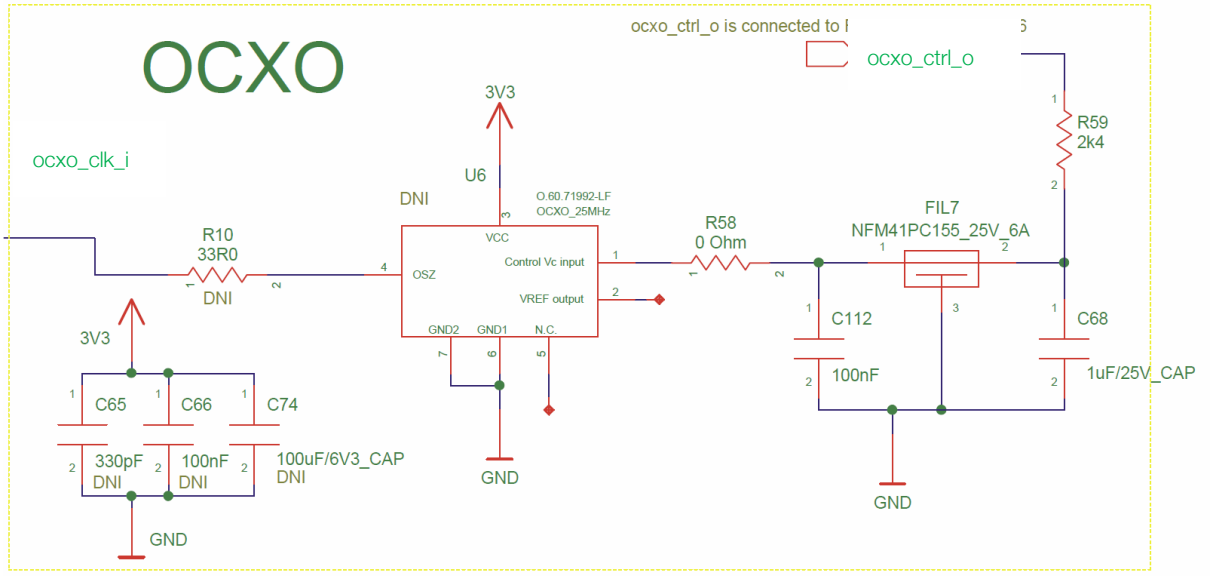

Figure 4 Connecting a voltage controlled OCXO to the syn1588® VIP

5 IP Core Interface

Signal Name	Direction	Description
gmii_gclk_i	In	125 MHz Clock from PHY See note (3)
gmii_txclk_i	In	GMII transmit clock See note (3)
gmii_txd_o<7:0>	Out	GMII transmit data to PHY See note (3)
gmii_txen_o	Out	GMII transmit enable See note (3)
gmii_txerr_o	Out	GMII transmit error See note (3)
gmii_rxclk_i	In	GMII receive clock See note (3)
gmii_rxd_i<7:0>	In	GMII receive data See note (3)
gmii_rxdv_i	In	GMII receive data valid See note (3)
gmii_rxerr_i	In	GMII receive error See note (3)
gmii_coll_i	In	GMII collision See note (3)
gmii_crs_i	In	GMII carrier sense See note (3)
gmii_gtx_clk_o	Out	GMII gigabit clock out See note (3)
gmii_mdio_clk_o	Out	MDIO clock out See note (3)
gmii_mdio_data_b	InOut	MDIO data See note (3)
gmii_reset_n_o	Out	PHY reset See note (3)
onepps_o	Out	one pulse per second output
frequency_o	Out	one frequency output
event_i	In	event input
insync_o	Out	in-sync output signal (high active)
uart_txd_o	Out	UART transmit data
uart_rxd_i	In	UART receive data
i2c_sda_b	InOut	Serial data
i2c_scl_o	Out	Serial clock
layersel_i	In	Select IEEE-1588 Layer 2 or Layer 3 mode See note (1)
mode_sw_i<2:0>	In	Mode of operation signals. See note (2)
sys_clk_i	In	25 MHz system clock input
reset_n_i	In	asynchronous reset signal (low active)
reset_n_o	Out	re-configuration signal from the watchdog unit (low active)
ocxo_clk_i	In	Optional OCXO clock input
ocxo_ctrl_o	Out	PWM output to OCXO control input AND clock output to SPI flash connected
spi_rxd_i	In	SPI flash read data
spi_txd_o	Out	SPI flash write data
spi_cen_o	Out	SPI flash chip enable (low active)

Table 1:syn1588 VIP_top IP Core interface signals

Signal Name	Direction	Description
gmii_gclk_i	In	125 MHz Clock from PHY See note (3)
gmii_txclk_i	In	GMII transmit clock See note (3)
gmii_txd_o<7:0>	Out	GMII transmit data to PHY See note (3)
gmii_txen_o	Out	GMII transmit enable See note (3)
gmii_txerr_o	Out	GMII transmit error See note (3)
gmii_rxclk_i	In	GMII receive clock See note (3)
gmii_rxd_i<7:0>	In	GMII receive data See note (3)
gmii_rxdv_i	In	GMII receive data valid See note (3)
gmii_rxerr_i	In	GMII receive error See note (3)
gmii_coll_i	In	GMII collision See note (3)
gmii_crs_i	In	GMII carrier sense See note (3)
gmii_gtx_clk_o	Out	GMII gigabit clock out See note (3)
gmii_mdio_clk_o	Out	MDIO clock out See note (3)
gmii_mdio_data_b	InOut	MDIO data See note (3)
gmii_reset_n_o	Out	PHY reset See note (3)
onepps_o	Out	one pulse per second output
frequency_o	Out	one frequency output
event_i	In	event input
insync_o	Out	in-sync output signal (high active)
uart_txd_o	Out	UART transmit data
uart_rxd_i	In	UART receive data
i2c_sda_b	InOut	Serial data
i2c_scl_o	Out	Serial clock
layersel_i	In	Select IEEE-1588 Layer 2 or Layer 3 mode See note (1)
mode_sw_i<2:0>	In	Mode of operation signals. See note (2)
sys_clk_i	In	25 MHz system clock input
sys_syn1588_i	In	syn1588® hardware clock signal
sys_8051_i	In	8051 microprocessor clock signal
reset_n_i	In	asynchronous reset signal (low active)
reset_n_o	Out	re-configuration signal from the watchdog unit (low active)
ocxo_ctrl_o	Out	PWM output to OCXO control input AND clock output to SPI flash connected
spi_rxd_i	In	SPI flash read data
spi_txd_o	Out	SPI flash write data
spi_cen_o	Out	SPI flash chip enable (low active)

Signal Name	Direction	Description
link_o	Out	Ethernet network link established (high active)
clockid_o<63:0>	Out	Clock Identifier of the syn1588® node
syn1588time_o<31:0>	Out	syn1588® hardware clock: actual seconds
port8051_o<28:0>	Out	8051 processor: output port signals
port8051_i<11:0>	In	8051 processor: input port signals

Table 2:syn1588 VIP_core IP Core interface signals

6 syn1588® VIP Evaluation Board

Oregano Systems offers a fully functional reference board to test drive the syn1588® VIP IP Core. Customers may receive all design data (board schematic, layout data, bill of material) of this reference board enabling them to easily adapt this design to their specific needs.

7 Software

No user supplied software is required for the syn1588® VIP device to operate, since everything needed is already integrated into the IP core's internal memories.

Only if the user wishes to gather status information about the nodes in layer 3 mode a program is available from Oregano Systems to access these data via the PTP management interface.

Furthermore if a GPS timing receiver is connected to the serial interface and the event input, the embedded SW will automatically detect the GPS timing information on that node and switch to the master state with the according clock stratum. If the connection to the GPS receiver is lost for more than two consecutive sync intervals, the node automatically switches back to normal (i.e. non-GPS) operation.

This capability allows a set of syn1588® VIP IP core's to replace GPS receivers by distributing timing information of a single GPS receiver across a LAN.

8 Further Information

You are looking for further information not included in this datasheet? Please contact Oregano Systems support! We will be pleased to provide you all the required information.

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